Ryerson University
Department of Electrical and Computer Engineering
COE 818–Advanced Computer Architecture

Midterm Test **March 1, 2013**

Name: _____ **Student Number:** _____

Time limit: 1 hour 50 min Examiners: N. Mekhiel

Notes:

a) Closed book.
b) No calculators.
c) Answer all questions **in the space provided**.

Q1-Assume the following C code :- (total=15 marks)

```
for(i=0; i<=1000; i++) {
                        A[i] =B[i]*X + 1;
                      }
```

• A- Convert the C code to MIPS Assembly code assume all variables are FP. (5 MARKS)

Each mistake -1

```
Loop: LD F1, 0(R1) ; B[i]
      MULT F2, F1, F3 ; B[i]*X
      ADDI F4, F2, #1 ;
      SD F4, 0(R2) ;
      ADDI R1, R1, #8
      ADDI R2, R2, #8
      SUB R3, R4, R1
      BNZ R3, Loop
```

Name:_____ Section:_____

B-Find the memory bandwidth of the above MIPS code assuming A[i], B[i] and X are 64 bit FP (using MIPS I, R, J instructions). (5 marks)

	Instructions	Data
LD F1, 0(R1)	32 = 4B	64 = 8B
MULT	4B	0
ADDI	4B	0
SD	4B	8B
ADDI	4B	0
ADDI	4B	0
SUB	4B	0
BNZ	4B	0

$$= \frac{8X4 + 8X2}{8 \text{ cycles}} = 6\ B/\text{cycles}$$

C-Find if it is a good idea to implement a new instruction that could replace two instructions: Multiply and Increment by one instruction as:
MULTI F1, F2, F3; means F1=F2*F3 + 1
Use the above code and assume that the processor speed will be reduced to 80% of original speed when the new instruction is implemented. Assume each instruction takes 1 clock cycle. (5 marks)

without new instruction = 8 x 1000 X 1
= 8000 cycles

with new instruction = 7 * 1000 X $\frac{10}{8}$
= 8.700 slower

Name:_____ Section:_____

Q2- (total = 10 marks)

A- Find if the following accesses are aligned or not assuming R1=1000 :- (4 MARKS)

- LB R2, 11(R1); Load a byte

  1011 mod 1 = 0 aligned

- LH R2, 17(R1); Load half word

  1017 mod 2 = 1 not aligned

- LW R2, 18(R1); Load a word

  1018 mod 4 = 2 not aligned

- LD F2, 100(R1); Load double word

  1103 mod 8 = 6 not aligned

$$8 \overline{)\,1103} \quad 137$$
$$8$$
$$30$$
$$24$$
$$63$$

B- How does the architecture deal with nonaligned accesses (2 MARKS)

- two memory accesses
- need alignment network inside processor

C-How can the compiler optimize performance of general purpose register LD/SD ISA. (2 marks)

- assign variables to registers using graph coloring
- rescheduling to get rid of hazards
- minimize code size
- use fast instructions

Name:_____ Section:_____

D-List advantages and disadvantages of using the following options in ISA:- (2 marks)

- Using 16 bits rather than 32 bits for immediate

16 bits cost less, small size instruction
32 bits more use, simplifys Compiler

- Using callee save versus caller save in subroutines

callee save more optimized for some application
caller: more conservative and reliable

Q3-PIPELINING:-

A-List all types of hazards in MIPS 5 Stages pipeline and give an example with code that could cause each type. (6 marks)

1- structural hazard between IM, DM

lw R1, 0(R2)
add R2, R1, R3

2- Data hazard

lw R1, 0(R2)
Add R3, R1, R3

result of lw not available until WB needed by Add in Decode

3- Control

beqz R1, Loop
- Instruction

Control in branch not defined until after Decode

Loop

Name:_____ Section:_____

C- Explain how MIPS pipeline handle FP operations and list all types of issues associated with this solution. (4 marks)

Using Multi-cycle operation in Execute
issues:- 1- Complicate EXCEPTION
2- Creates structural hazard
Two writes at same time
3- Creates WAW hazard

Q4-Show the timing of the following code sequence in MIPS pipeline assume forwarding, scheduling and branch uses delayed branch and all memory references are in cache ~~(FP Add takes 4 cycles)~~. (10 marks)

```
LOOP: LW R3, 0(R1)
      LW R4, 0(R2)
      ADD R5, R4, R3
      ADDI R6, R5, #1
      SW R6, 0(R1)
      ADDI R1, R1, #4
      ADDI R2, R2, #4
      SUBI R8, R7,R2
      BNZ R8, LOOP
```