Ryerson University
Department of Electrical and Computer Engineering
COE 818–Advanced Computer Architecture

Midterm Test **Feb 27, 2012**

Name: _____ **Student Number:** _____

Time limit: 1 hour 50 min Examiners: N. Mekhiel

Notes:

a) Closed book.
b) No calculators.
c) Answer all questions **in the space provided**.

TOTAL = 60

Q1-Assume the following C code :- (total=20 marks)

```
for(i=0; i<=1000; i++) {
                        A[i] =A[i] + S*B[i];
                      }
```

• A- Convert the C code to MIPS Assembly code. (5 marks)

```
    LW R5, 0(R5); S
LOOP: LW R1, 0(R2); A[i]
    LW R4, 0(R3); B[i]
    MULT R4, R5, R4; S*B[i]
    ADD R4, R4, R1;
    SW R4, 0(R2);
    ADDI R2, R2, #4
    ADDI R3, R3, #4
    SUB R7, R6, R2;
    bnz R7, LOOP
```

missing -½

Name:_____ Section:_____

B-Find the memory bandwidth of the above MIPS code assuming A[i], B[i] and S are 32 bit integers and are stored in memory. Assume op-code=1 byte, memory address is 4 bytes, immediate and displacement size= 2 bytes, and there are 64 registers. (5 marks)

	Inst.	Data
LW R5, 0(R6)	8+6+16+6 = 4.5 B	4B
Loop: LW R1, 0(R2)	= 4.5 B	4B
LW R4, 0(R3)	= 4.5 B	4B
MULT R4, R5, R4	8+6+6+6 = 3 1/4 B	0
ADD R4, R4, R1	" = 3 1/4 B	0
SW R4, 0(R2)	8+6+6+16 = 4.5 B	4B
ADDI R2, R2, #4	8+6+6+16 = 4.5 B	0
ADDI R3, R3, #4	8+6+6+16 = 4.5 B	0
SUB R7, R6, R2	8+6+6+6 = 3 1/4 B	0
BNZ R7, Loop	8+6+16 = 3 3/4 B	0
	40.5 B	12B

BW = 52.5 / 9 = 5.8 B/cycle

C-Calculate the memory bandwidth if a fixed instruction length is used. If the instruction is shorted than 4 bytes it uses a 4 byte. If the instruction is longer than 4 bytes, it uses two instructions of 4 bytes each and cost two processor accesses. (5 marks)

	Inst.	Data
LW R5, 0(R6)	8B	4B
Loop: LW R1, 0(R2)	8B	4B
LW R4, 0(R3)	8B	4B
MULT R4, R5, R4	4B	0
ADD R4, R4, R1	4B	0
SW R4, 0(R2)	8B	4B
ADDI R2, R2, #4	8B	0
ADDI R3, R3, #4	8B	0
SUB R7, R6, R2	4B	0
BNZ R7, Loop	4B	0
	56B	12B

BW = 68B / 14 = 4.85 B

Name:_____ Section:_____

D-Find if it is better for the performance to use the fixed instruction length assuming that the fixed instruction length uses 20% faster clock. (5 marks)

$T = 1 + 1000 \times 9 \approx 9000$ cycles ✓

$T_{Fixed} = \frac{(1 + 1000 \times 1A)*}{1.2} = 12000$ cycles

NO, it is not

Q2- (total = 10 marks)

A- Explain the Role of Compiler in optimizing the performance of applications. (3 marks)

- it assigns variables that are most frequently used To Registers To reduce memory Traffic
- schedule code To hide hazards
- evaluate expressions in any order. .
- Pick Fast Instructions
- hide branch latency

Name:_____ Section:_____

B-Explain why the compiler does not assign a data element referenced by a pointer to a register and give an example. (2 marks)

- aliasing problem, it could have different value (1)

*p = &a
R1 = a = 5
*p = 7 R1 a different (1)

C-Why compiler does not use callee saving and explain by giving example. (3 marks)

callee could call another routine that changes one of the variables that is not saved by callee
example: Program call Routine1, that does not use x Routine1 does not save x, if Routine1 calls Routine2, and Routine 2 changes x, then x in main Program will not be same when they return.

D- Explain the advantages and the disadvantages of adding an extra addressing mode to ISA. (2 marks)

- Advantages: better for Compiler, easy code.
- disadvantage: slower, more complicated

Q3- Pipelining (total=30 marks)

A-List all types of hazards in MIPS 5 stage Integer pipeline, and give example for the code that would cause each hazard. (6 marks)

(1) structural hazard:
lw F... (M) followed by ADD DE (E) this same memory
Fetch in one clock cycle operand

(2) data hazard
lw R1, 0(R3)
ADD R2, R1, R1
Data of current Instruction is not ready in time

(3) control hazard
BNZ R1, Loop
Fetch of next instruction is not known in time because of BTA not calculated and known

Name:_____ Section:_____

B- Explain why pipelining complicates handling exceptions by giving examples.
(4 marks)

1- could have Two exceptions in one clock

Fetch Instruction 2 could cause page fault,
Decode Inst 1 could have illegal Inst.

2- OUT of order exception

Fetch Inst 2 could cause page fault,
earlier than Inst 1 could cause Memory
page fault later
They must handle in order of their
occurance Inst 1 First, Then Inst 1 as
normal Pipelined

Name:_____ Section:_____

C-In the MIPS pipeline with multi-cycle floating point operations, give examples of the following.-
i-WAW Hazard (3 marks)

ADD F1, F2, F3,
LW F1, F4, F5

ii- A structural hazard that occur in MIPS floating multi-cycle pipeline (3 marks)

Two writes in same time

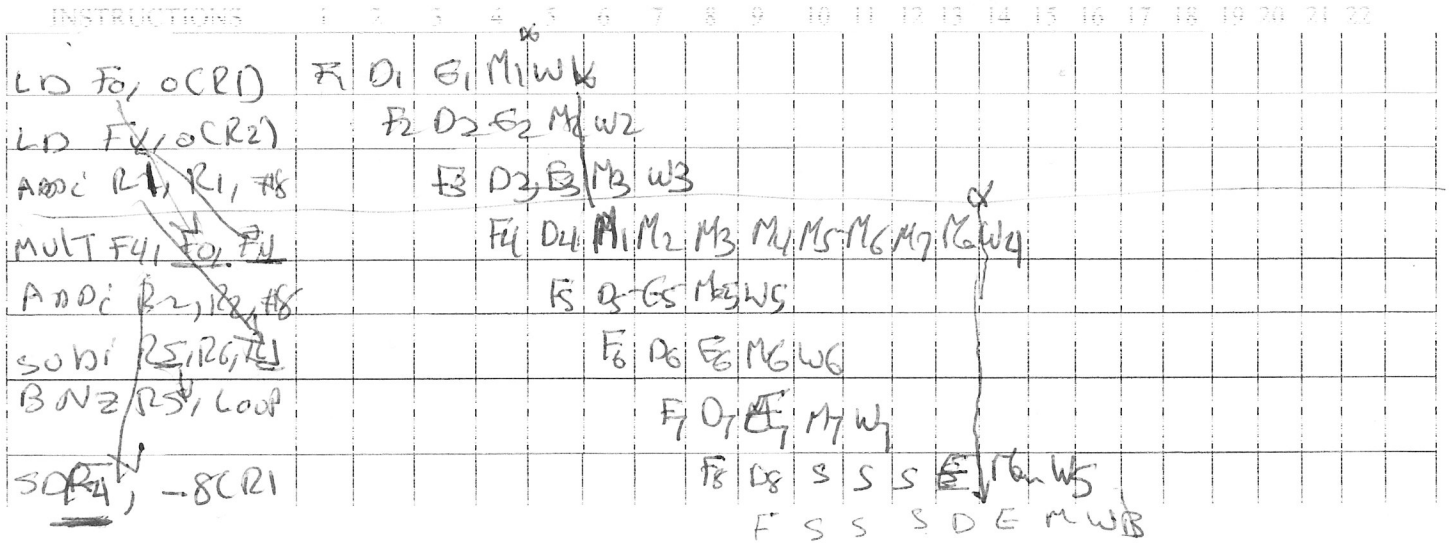
ADD F1, F2, F3 F I D A1 A2 A3 A4 M WB
~~OR R1, R2, R3~~ F D E M W
~~SUB R4, R5, R6~~ F D E M W B.
F D E M WB
LW F5, 0(R1)

or FP divider

D-Show the timing of the following code sequence in MIPS FP pipeline assume forwarding, scheduling and branch uses delayed branch and all memory references are in cache (FP Mult takes 7 cycles). (14 MARKS)

```
LOOP: LD F0, 0(R1)
      LD F4, 0(R2)
      Mult F4, F0, F4
      SD F4, 0(R1)
      ADDI R1, R1, #8
      ADDI R2, R2, #8
      SUBI R5, R6,R1
      BNZ R5, LOOP
```

Name:_____ Section:_____



11 cycles