COE 818 Final Exam , April 24 , 2006
Answer all questions in the available space
Total Marks = 100, Time=2 1/2 hours

1 Q1 (ISA=30 marks)

1.1 15 marks

Convert to MIPS Assembly, then find the performance (total time) of the following C code assuming:
1-ideal pipelining (no stalls and no start up time)
2- all instructions and data accesses are in cache (100% hit).
3-Processor speed = 1 GHz.

```
for(i=1; i<=512; i++)  {

   Y[i] =Y[i] + A*X[i];

                        }
\\
 (Assume A, X[i], Y[i] are 32 bits)
```

1.2 15 marks

Convert the above code to MIPS Instructions for Vector Processing, and find the performance in total time assuming the following:-
1- MIPS uses a Vector processor with fully pipelined function units and vector registers of 128 elements.
2-MIPS Vector processor runs at 1 GHz.
3-All instructions are in cache (100% hit), data accesses use interleaved memory for load/store and are fully pipelined with no stalls.

2 Q2 (Advanced Pipelining= 25 marks)

2.1 scheduling=15 marks

The following code runs in DLX architecture, FP ALU op has latency= 3 cycles, FP ALU op to SD latency= 2 cycles and LD latency = 1 cycle.

```
loop:  LD     F0, 0(R1)  ; Load X[i]
       LD     F4, 0(R2) ; Load Y[i]
       ADDD   F6, F4, F0; X[i]+Y[i]
       SD     0(R2), F6
       SUBI   R1,R1,#8
       SUBI   R2,R2,#8
       BNEQZ  R1, loop
```

Find the following:

- All types of hazards.

- The performance of the above (cycles per loop).

- Use loop unrolling 3 times and schedule the code to improve performance. Find the performance of the code.

2.2 multiple-issue=10 marks

In the above example of 2.1 , assume that the DLX uses a superscalar to issue two instructions on each clock (1 Int, 1 FP). Write the code for the superscalar and find the performance in cycles per loop(unroll loop 3 times).

3 Q3 (Advanced Pipelining= 15 marks)

The following code runs in a DLX architecture with scoreboarding, FP ADD op has latency= 2 cycles, FP MULTD latency= 8 cycles, LD latency = 1 cycle, and 2 ADD/SUB function units.

```
LD     F2, 0(R1)  ; Load X[i]
MultD  F4,F0, F2   ; aX[i]
ADDD   F10, F4, F8
SUBD   F8,F8,F0
SD     F8, 0(R1)
```

- Find the Scoreboard instruction status at the end of code execution.

4 Q4 (Multiprocessor Systems= 30 marks)

4.1 =4

Compare the advantages and disadvantages of write invalidate versus write update for multiprocessor systems.

4.2 =3

Explain how does multiprocessor system with two level cache maintain coherency.

4.3 =8

Assume a shared memory multiprocessor system that uses the write invalidate snooping coherency protocol. Find the state of the cache block after each of the following operations:-

- Processor read miss to a private block in its cache

- Processor write hit to invalid block in its cache

- Processor write miss to shared block in its cache

- Bus read operation hit to a private block in cache

4.4 =15

In a shared memory multiprocessor system assume the following:-
1-the system uses the write invalidate coherency protocol.
2-All processor's speed = 1 GHz. Processor P1 has R1= 100 and Processor P2 has R3= 200. All other registers =0.
3-Each processor uses a direct mapped cache. The cache size = 512 Kbytes, block size= 8 bytes. The cache speed is the same as processor speed.
4-The bus width is 8 bytes and bus latency and waiting time = 200 ns. Memory latency = 100 ns.

The above system is executing the following events:-

step#	P1	P2	OUTCOME in C1 and C2, TIME
1	LW R4, 100(R1)	--------	----------
	----------	----------	----------
2		LW R5, 104(R1)	----------
	----------	----------	----------
3	SW 100(R1), R7	---------	----------
	----------	----------	----------
4	----------	LW R16,100(R1)	----------
	----------	----------	----------
5	LW R12, 100(R1)	----------	----------
	----------	----------	----------

Find the outcome in processor caches (C1,C2) and time required to perform each event in the above code (state, processor, bus, memory operations and cost in time).