COE 818 Final Exam , April 24 , 2006
Answer all questions in the available space
Total Marks = 100, Time=2 1/2 hours

1 Q1 (ISA=30 marks)

1.1 15 marks

Convert to MIPS Assembly, then find the performance (~~number of cycles~~ Time) of the following C code assuming:
1-ideal pipelining (no stalls and no start up time)
2- all instructions and data accesses are in cache (100% hit).
3-Processor speed = 1 GHz.

```
for(i=1; i<=512; i++)  {

   Y[i] =Y[i] + A*X[i];

                        }
\\
 (Assume A, X[i], Y[i] are 32 bits)
```

Loop: Lw R2, 100(R1) ; load X(i)
lw R3, 5000(R1); load Y(i)
MulT R4, R2, R6; R6 = A (1c)
Add R7, R4, R3
Sw R7, 5000(R1)
subi R1, #4 ;
bnz R1, Loop

T = 512 X 7 X 1 ns = 3.584 µs (5)

1.2 15 marks

Convert the above code to MIPS Instructions for Vector Processing, and find the performance in ~~clock cycles~~ time assuming the following:-
1- MIPS uses a Vector processor with fully pipelined function units and vector registers of 128 elements.
2-MIPS Vector processor runs at 1 GHz.
3-All instructions are in cache (100% hit), data accesses use interleaved memory for load/store and are fully pipelined with no stalls.

```
LOOP LDV V1, 100(R1)  ; X[i]      ; 128
     LDV V2, 5000(R1) ; Y[i]      ; 128
     MULT V3, V1, F0  ; A X       ; 128
     ADDV V4, V3, V2  ; AX + Y    ; 128
     SV V4, 5000(R1)
     subi R1, #4x128
              (512)
     bnz R1, LOOP
```

10

$T = 4 \times (128 + 128 + 128 + 128 + 128 + 2) \times 1\,ns$

$= 4 \times 642\,ns = 2568\,NS$

5

2 Q2 (Advanced Pipelining= 25 marks)

2.1 scheduling=15 marks

The following code runs in DLX architecture, FP ALU op has latency= 3 cycles, FP ALU op to SD latency= 2 cycles and LD latency = 1 cycle.

```
1- loop: LD     F0, 0(R1)   ; Load X[i]
2-       LD     F4, 0(R2)   ; Load Y[i]
3-       ADDD   F6, F4, F0  ; X[i]+Y[i]
4-       SD     0(R2), F6
5-       SUBI   R1,R1,#8
6-       SUBI   R2,R2,#8
7-       BNEQZ  R1, loop
```

Find the following:

- All types of hazards.

RAW (1)→(3), (2)→(3), (3)→(4), (5)→(7)

5

Control BNEQZ

- The performance of the above (cycles per loop).

5

```
Loop: LD   F0, 0(R1)      1
      LD   F4, 0(R2)      2
      ADD  F6, F4, F0     3
      SD   0(R2), R6      4
      SUBI R1, R1, #8     5
      SUBI R2, R2, #8     6
      BNEQZ R1, loop      7
```

stall (5), (6)

stall 8

stall 9

stall 10

stall Control 11, 12

12 cycles / Loop

1D array

- Use loop unrolling 3 times and schedule the code to improve performance. Find the performance of the code.

(5)

```
Loop: LD F0, 0(R1)
      LD F1, -8(R1)
      LD F3, -16(R1)
      LD F4, 0(R2)
      LD F8, -8(R2)
      LD F10, -16(R2)
      ADD F6, F4, F0
      ADD F12, F8, F1
      ADD F14, F3, F10
      SD 0(R2), F6
      SUBI R1, R1, #24
      SUBI R2, R2, #24
      SD +16(R2), F12
      BNZ R1, Loop
      SD -8(R2), F14
```

cycles/loop = $\frac{15}{3}$ = 5 cycles

2.2 multiple-issue=10 marks

In the above example of 2.1 , assume that the DLX uses a superscalar to issue two instructions on each clock (1 Int, 1 FP). Write the code for the superscalar and find the performance in cycles per loop. (Unroll Loop 3 Times)

10

	Int.	FP
loop ①	LD F0, 0(R1)	
②	LD F4, -8(R2)	
③	LD F1, -8(R1)	~~ADD F6, F4, F0~~
④	LD F8, -8(R2)	ADD F6, F4, F0
⑤	LD F3, -16(R1)	
⑥	LD F10, -16(R2)	ADD F12, F8, F1
⑦	SD F6, 0(R2)	ADD F14, F3, F10
⑧	SUBI R2, R2, #24	
⑨	SUBI R2, R2, #24	
⑩	SD +16(R2), F12	
⑪	BNZ R1, loop	
⑫	SD +8(R2), F14	

3 ⑤ ⑤ ⑤

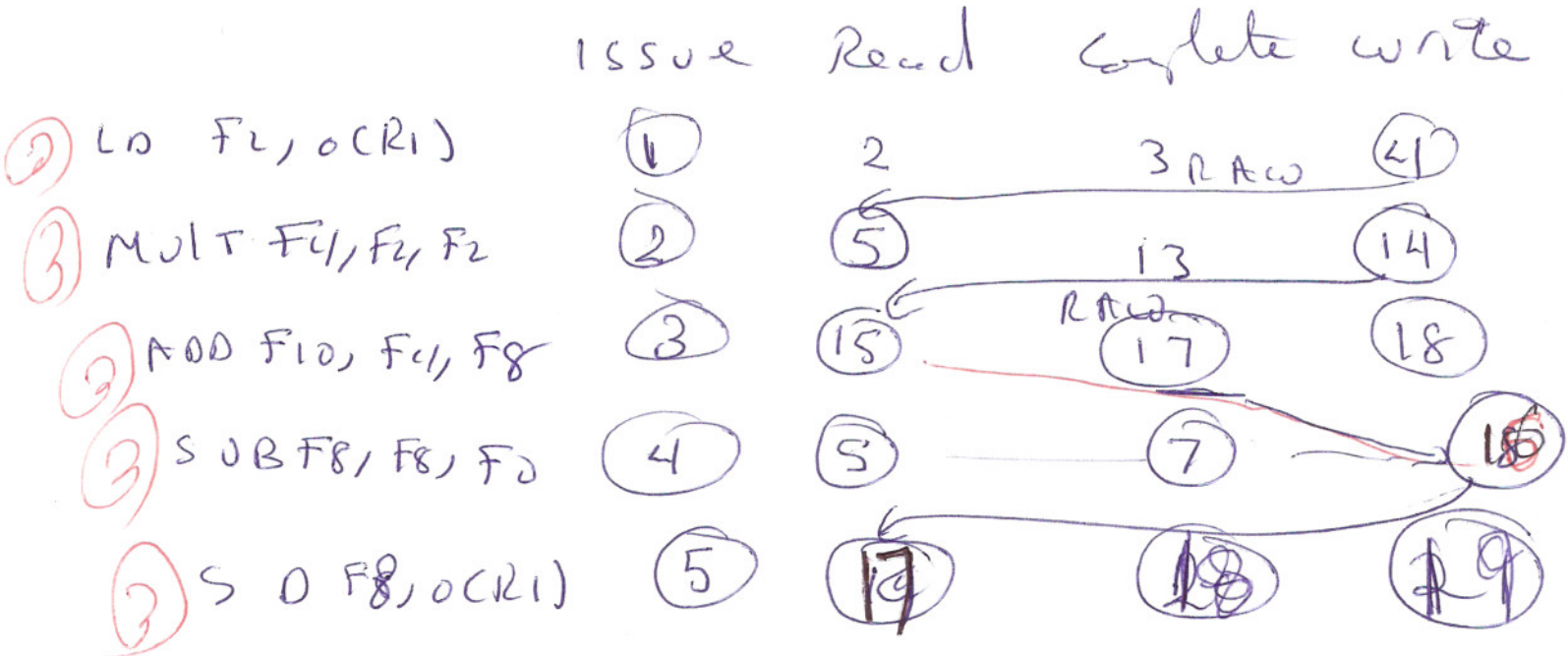
Performance = $\frac{12}{3}$ = 4 cycles / loop

3 Q3 (Advanced Pipelining= 15 marks)

The following code runs in a DLX architecture with scoreboarding, FP ADD op has latency= 2 cycles, FP MULTD latency= 8 cycles, LD latency = 1 cycle, and 2 ADD/SUB function units.

```
LD      F2, 0(R1)   ; Load X[i]
MultD   F4,F0, F2    ; aX[i]
ADDD    F10, F4, F8
SUBD    F8,F8,F0
SD      F8, 0(R1)
```

- Find the Scoreboard instruction status at the end of code execution.



4 Q4 (Multiprocessor Systems= 30 marks)

4.1 =4

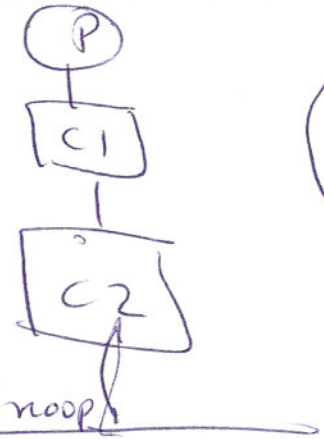
Compare the advantages and disadvantages of write invalidate versus write update for multiprocessor systems.

write invalidate: uses bus only once for multiple writes (bus utilization is better)

write update: uses bus each time needs to update, sending data on bus, but has faster read after write update (fast Read)

4.2 =3

Explain how does multiprocessor system with two level cache maintain coherency.



- Inclusion, each block of C1 is in C2. only C2 snoops on bus, if block is not in C1, need not to invalidate it in C1, but if it is in C1, needs vertical invalidation

4.3 =8

Assume a shared memory multiprocessor system that uses the write invalidate snooping coherency protocol. Find the state of the cache block after each of the following operations:-

- Processor read miss to a private block in its cache

shared

- Processor write hit to invalid block in its cache

private

- Processor write miss to shared block in its cache

private

- Bus read operation hit to a private block in cache

shared

4.4 =15

In a shared memory multiprocessor system assume the following:-
1-the system uses the write invalidate coherency protocol.
2-All processor's speed = 1 GHz. Processor P1 has R1= 100 and Processor P2 has R3= 200. All other registers =0.
3-Each processor uses a direct mapped cache. The cache size = 512 Kbytes, block size= 8 bytes. The cache speed is the same as processor speed.
4-The bus width is 8 bytes and bus latency and waiting time = 200 ns. Memory latency = 100 ns.

The above system is executing the following events:-

step#	P1	P2	OUTCOME, TIME
1	LW R4, 100(R1)	--------	read miss, shared C1
	Time = 200 + 100 + 1		= 301
2		LW R5, 104(R1)	read miss, shred
	from C1 = 200+1+1 =		202
3	SW 100(R1), R7	--------	write hit,
	Private C1, invalidate C2	T = 200+1+1	
4	----------	LW R16,100(R1)	read, invalid cop
	shared C1	T = 200+1+1	
5	LW R12, 100(R1)	----------	read hit = 1 cycle
	shared C1, C2		

Find the outcome and time required to perform each event in the above code (state, processor, bus, memory operations and cost in time).