COE 818 Final Exam , April 17, 2012

Total Marks = 100, Time=2 1/2 hours

Answer all questions

Name_____

Q1 (ISA=20 marks)
Q1-1 (10 marks)
Find the performance of the following C code in a MIPS architecture assuming:-
- Ideal pipelining (no stalls and no start up time)
- Assume that instructions and data cache have 100% hit rate.
- MIPS has a SIMD unit similar to MMX.
- Processor and Cache speed = 1 GHz.
- the C Code is:-

```
for(i=1; i<=1024; i++) {
Y[i] =A +Y[i]* X[i];
}
```

(Assume X[i]= Y[i]= 16 bits)

F1

A(0)	A(1)	A(2)	A(3)

```
Loop: LD F1, 0(R1);   X[i]
      LD F2, 0(R2);   Y[i]
      MULT F3, F1, F2;
      ADD F4, F3, F5
      SD F4, 0(R2)
      ADDI R1, R1, #8
      ADDI R2, R2, #8
      SUB R4, R3, R1
      bnz R4, Loop
```

$$T = \frac{1024}{4}(9\ ns) = 256 \times 9 = 2304\ ns$$

Q1.2 (10 marks)

Find the performance of the above code assuming the following:-
- MIPS uses a Vector processor with fully pipelined function units and vector registers of 64 elements.
- MIPS runs at 1 GHZ.
- All instructions are in cache (100% hit), data accesses use interleaved memory for load/store and are fully pipelined with no stalls.

```
Loop LV V1, a(R1)      64 ns
     LV V2, o(R2)      64 ns
     MulV V3, V1, V2   64 ns
     Add V4, F1, V3    64 ns
     SV V4, o(R2)      64 ns
     Addi R1, R1, #128
     Addi R2, R2, #128
     Sub R4, R3, R1
     Bnz R4, Loop
```

$$T = \frac{1024}{64} * (5 \times 64 + 4) = 16 * (324)$$

$$T = 5{,}184 \text{ ns}$$

Q2 (Advanced Pipelining= 25 marks)
Q2.1 scheduling=15 marks
The following code runs in MIPS architecture, FP ALU op has latency= 3 cycles, FP ALU op to SD latency= 2 cycles and LD latency = 1 cycle.

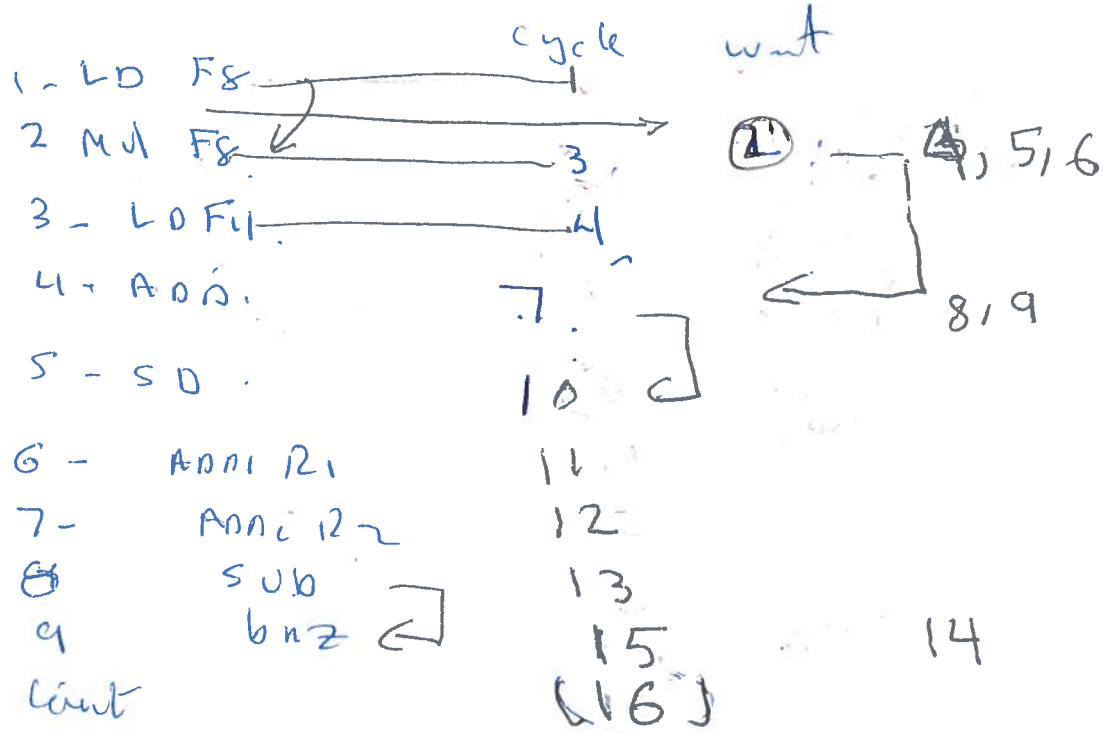
```
1- loop: LD F8, 0(R1) ; Load X[i]
2 -      MultD F8,F8, F2 ; aX[i]
3 -      LD F4, 0(R2) ; Load Y[i]
4 -      ADDD F6, F4, F8; aX[i]+Y[i]
5 -      SD 0(R2), F6
6 -      ADDI R1,R1,#8
7 -      ADDI R2,R2,#8
8 -      SUB R7, R6, R1
9 -      BNEQZ R7, loop
```

Find the following:

- All types of hazards. (5 Marks)

RAW: 1-2, 2-4, 4-5, 6-8, 8-9
Control 9
WAW: 1, 2

- The performance of the above (cycles per loop). (5 Marks)



• Use loop unrolling 4 times and schedule the code to improve performance. Find the performance of the code. (5 Marks)

```
LD F8, 0(R1)        1
LD F9, +8(R1)       2
LD F10, +16(R1)     3
LD F11, +24(R1)     4
MUL F8, F8, F2      5
MUL F9, F9, F2      6
MUL F10, F10, F2    7
MUL F11, F11, F2    8
LD F4, 0(R2)        9
LD F12, +8(R2)      10
LD F13, +16(R2)     11
LD F14, +24(R2)     12
ADD F8, F4, F8      13
ADD F14, F12, F9    14
ADD F15, F13, F10   15
ADD F16, F14, F11   16
SD F8, 0(R2)        17
SD F14, +8(R2)      18
ADDI R1, R1, #32    19
ADDI R2, R2, #32    20
SUBI R7, R6, R1     21
SD F15, +16(R2)     22
BNZ R7, LOOP        23
SD F16, -8(R2)      24
```

$\frac{24}{4} = 6$

Q2.2 multiple-issue=10 marks

In the above example with unrolling loop 4 times, assume that MIPS uses a superscalar to issue two instructions on each clock (1 Int, 1 FP). Write the code for the superscalar and find the performance in cycles per loop.

LD F8	1	
LD F9	2	
LD F10	3	Mul F8
LD F11	4	Mul F9
LD F4	5	Mul F10
LD F12	6	Mul F11
LD F13	7	ADD F5, F4, F8
LD F14	8	ADD F14, F12, F9
	9	ADD F15, F13, F10
SD F5	10	ADD F16, F14, F11
SD F4	11	
ADDi	12	
ADDi	13	
Subi	14	
SD	15	
bnz	16	
SD	17	

or

16 cycles = 4 or

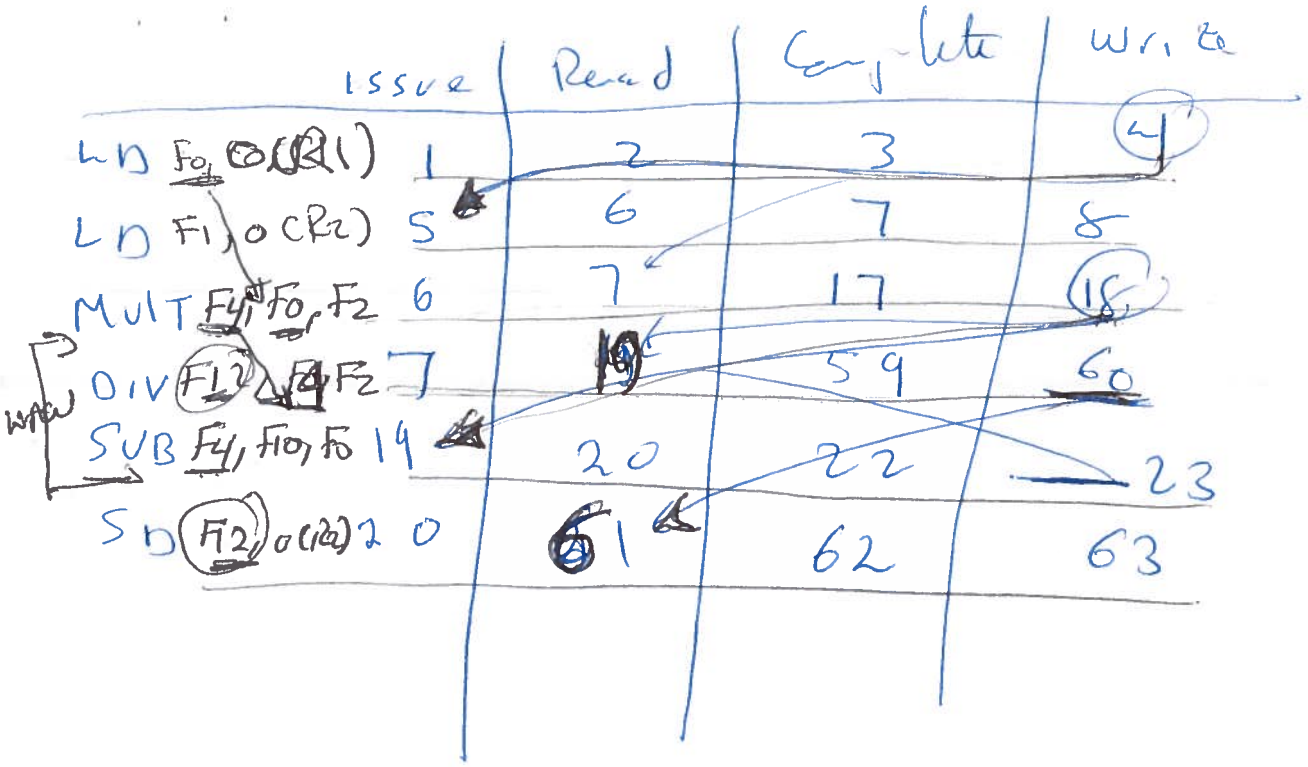
could schedule ADDi in cycle 9 and will be 16 cycles only

Q3 (Advanced Pipelining= 25 marks)

The following code runs in a MIPS architecture with Scoreboarding, FP ADD op has latency= 2 cycles, FP MULTD latency= 10 cycles, Divide latency= 40 cycles, LD latency = 1 cycle, and 1 ADD/SUB function unit . (15 Marks)

```
LD F0, 0(R1) ; Load X[i]
LD F1, 0(R2) ; Load Y[i]
MultD F4,F0, F2 ; aX[i]
Div F12, F4, F1
SUBD F4,F10,F0
SD F12, 0(R1)
```

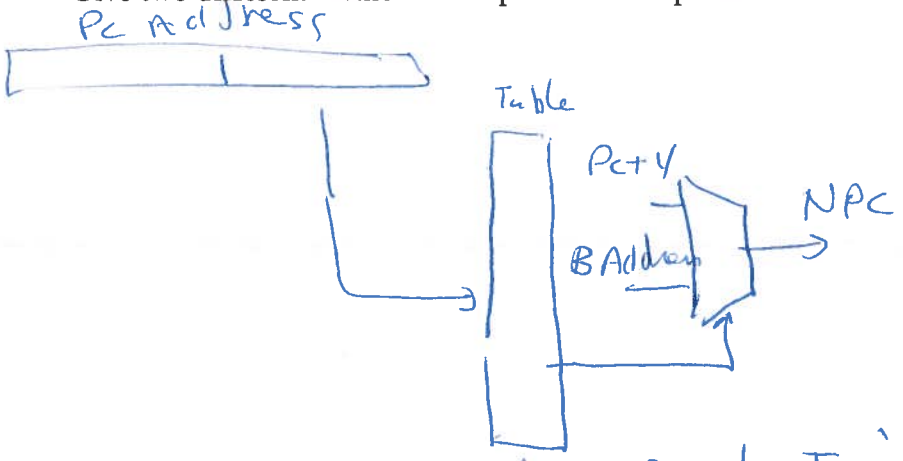
• Find the Scoreboard instruction status at the end of code execution.



Q3.2 (4 Marks)
Why control dependency must be preserved.

- For correct data flow
- For correct exception

Q3.3 (6 Marks)
Draw a block diagram of branch predictor.
Give two different methods to improve branch prediction accuracy.



- use 2 bits prediction
- use global address branches

Q4 -(Multiprocessor Systems= 30 marks)
Q4.1-(Marks =3)
Give the reasons for why multiprocessor system cannot be made scalable.

- Communication
- Serial Code

Q4.2-(Marks =4)
Explain and give example of false sharing in cache coherency protocols.

block in cache is multiple words, and all words are invalidated even not written to

- P_1 read X_1
- P_2 read X_2 (X is shared)
- P_1 writes to X_1 (P_2 INV X_1, X_2)
- P_2 Reads X_2 X_2 is invalid although it has not changed

Q4.3-(Marks =8)
Assume a shared memory multiprocessor system that uses the write invalidate snooping coherency protocol. Find the state of the cache block after each of the following operations:-

• Bus read to private block in cache

shared

• Processor read miss to invalid block in cache

shared

• Processor write miss to private block in cache

private

• Bus write operation hit to invalid block in cache

Invalid

Q4.4-(Marks =15)
In a shared memory multiprocessor system assume the following:-
• the system uses the write invalidate coherency protocol.
• All processor's speed = 1 GHz. Processor P1 has R1= 400 and Processor P2 has R3= 480. All other registers =0.
• Each processor uses a direct mapped cache. The cache size = 512 Kbytes, block size= 32 bytes. The cache speed is the same as processor speed.
• The bus width is 8 bytes and bus latency and waiting time = 100 ns.
• Memory latency = 200 ns.
The above system is executing the following events:-

step#	P1	State	Time	P2	State	Time
1	LW R4, 80(R1)	shared,				
				From memory		= 100+200+4 = 304
2				LW R5, 4(R3)		
				shared		100+1 = 101+4 From C1 +4 = 105
3				SW R7, 4(R3)		
	INValid			private, 100+1 = 101		
4	SW R8, 80(R1)					
	private 101			INvalid		
5	LW R16, 0(R3)					
	shared T= 304 from memory					