5.07 - 52 4o

Digital Systems Engineering COE 758
Midterm Test, Date: October 29, 2009

Time: 1 hour and 50 Minutes
Each question=10 marks
Answer all the following questions

Student name _____

Q1-Briefly compare the ~~advantages and disadvantages of the following~~:-
a-Low order address ~~bank mapping versus~~ high order address in DRAM
b-Using a capacitor versus transistors as a storage element in memory
c-Using unified cache versus separate D and I cache for L1
d-Using LRU versus random policy in cache
e-Large versus small page size in Virtual memory

(10)

(2) a - low order ~~address~~ bank mapping is useful for Precharge interleaving / not for fast page
high order address interleaving is useful for Fast page mode

(2) b - Capacitor is small, cost effective but needs ~~Precharge~~ complex circuit
Transistors - fast, no need for refresh

(2) c - Unified has better hit rate, D, I separate cache do not cause a ~~Data~~ pipeline hazard

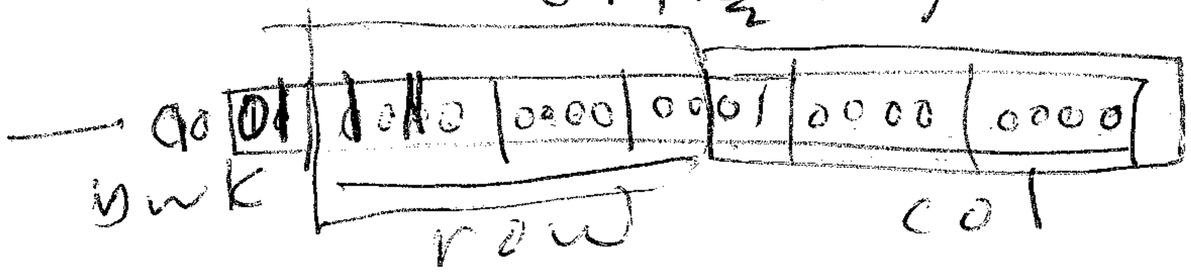
(2) d - LRU gives better hit rate
Random is simpler to implement

(2) e - Large page size reduce Page Table size, overhead of Trans for
Small Page - reduce ~~Fragmentation~~ Fragmentation

Q2-i-A memory system uses 4-Banks with fast page and high order address bank mapping implemented with 1MX8 DRAM modules.

Find the page hit rate for the following sequence of addresses given in hex: 01A00100, 02A00200, ~~01A00B0, 02A00300, 01A00100, 02A00500~~ (find bank , row of each access)

01A00100, 02A00200, 01A00B0, 02A00300
01A00100, 02A00500



bnk #1 row 1010-000000 miss

02A00200

col

bnk=2 row = 1010 000000 miss

01A00B0

bnk=1, row = 1010 000000 hit

02A00300

bnk=2 row= 1010 000000 hit

01A00100

bnk=1 row = 1010 000000 hit

02A00500

bnk 2 row 1010 000010 miss

hit rate = 3/6 = 50%

Q2-ii-Find average access time to DRAM that uses two banks precharge interleaving assuming a bank conflict=20%, precharge time(Trp)= 4 cycles, row to column time (TRC)= 2 cycles, and column access time (Tcac)= 2 cycles.

T = .80 * 4 cycles + .2 * 8

= 3.2 + 1.6 = 4.8 cycles

4

Q3-i -A direct mapped Cache system with total size = 32 bytes and the block size = 4 bytes. For the following sequence of accesses, find the hit rate:
8, 40, 10, 17, 81, 16, 11, 19

Memory address	Memory blk #	cache blk #	hit/miss
8	2	2	miss
40	10	2	miss, out
10	2	2	miss
17	4	4	miss, out
81	20	4	miss, out
16	4	4	miss
11	2	2	hit
19	4	4	hit

	3	2	1	0
0				
1	7	6	5	4
2	—	—	—	8

	31	30	29	28
7				

$\frac{2}{8} = 25\%$

Q3- ii-Compare the performance of a direct mapped cache to a two way set associative cache assuming the following:-

-direct mapped cache uses a block size= 16 B, has a miss rate= 8%, speed = 10 ns.

-two way associative has a block size = 8 B, miss rate= 5%, and speed = 15 ns.

-Main memory access time = 60 ns, and bus bandwidth = 5 GB/S 500 MB/S

(2) $T_{directmapped} = 10 + .08 \times (60 + \frac{16}{.5})$

$= 10 + .08 \times (92)$

$= 10 + 7.36 = 17.36 ns$

(2) $T_{2way} = 15 + .05(60 + \frac{8}{.5})$

$= 15 + .05 \times 76$

$= 18.8 ns$

slower

Q4-i-A 16 KByte V.M. space, if main memory size = 8 KByte, page size= 2 KByte and the content of page table starting from base is 0, 4, 6, 7, 5, 1, 3, 2 and MSB ~~is~~ used as valid bit. ~~Find~~ % page ~~hit for the following~~ (~~not in~~ sequence) accesses: 580, 1078, 2750, 2040, 5180, 7050

Table

VP		
0	0	0 0
1	1	0 0
2	1	1 0
3	1	1 1
4	1	0 1
5	0	0 1
6	0	1 1
7	0	ϕ 0

0	VP1
1	VP4
2	VP2
3	VP3

580 - VP = ϕ

1078 ÷ 2K = ϕ VP ϕ hit

2750 ÷ 2048 = 1 VP 1 hit

2040 ÷ 2048 = ϕ VP ϕ = hit

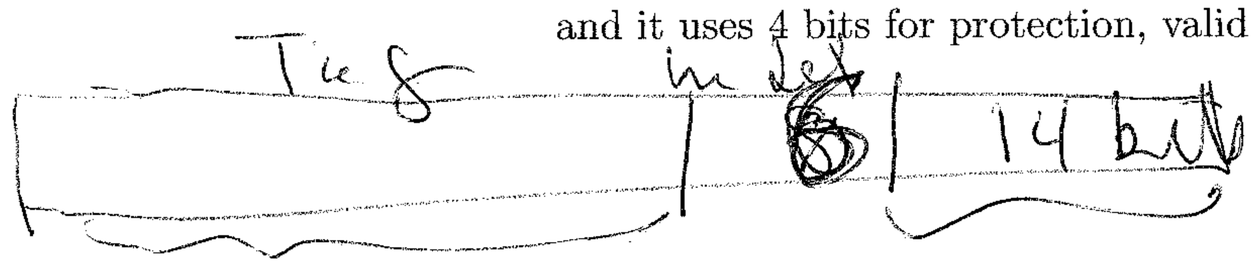
5180 ÷ 2048 = 2 VP2 = hit

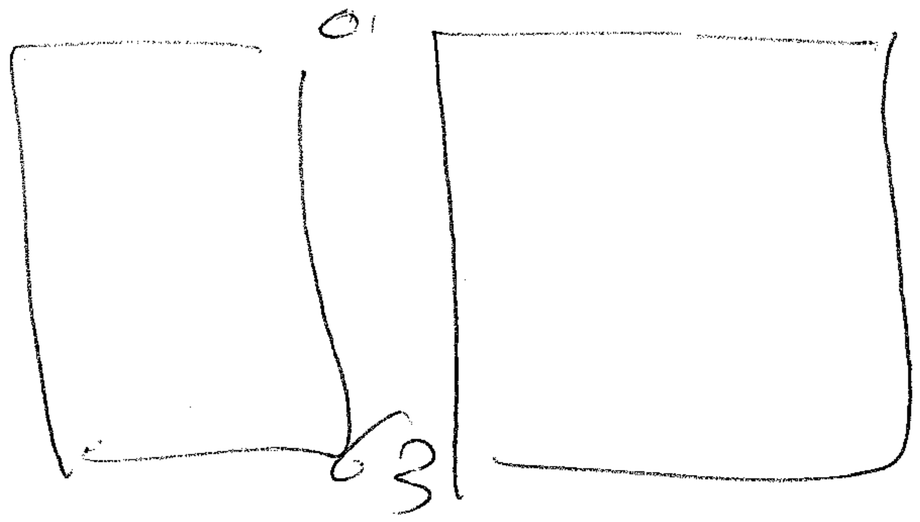
7050 ÷ 2048 = 3 hit

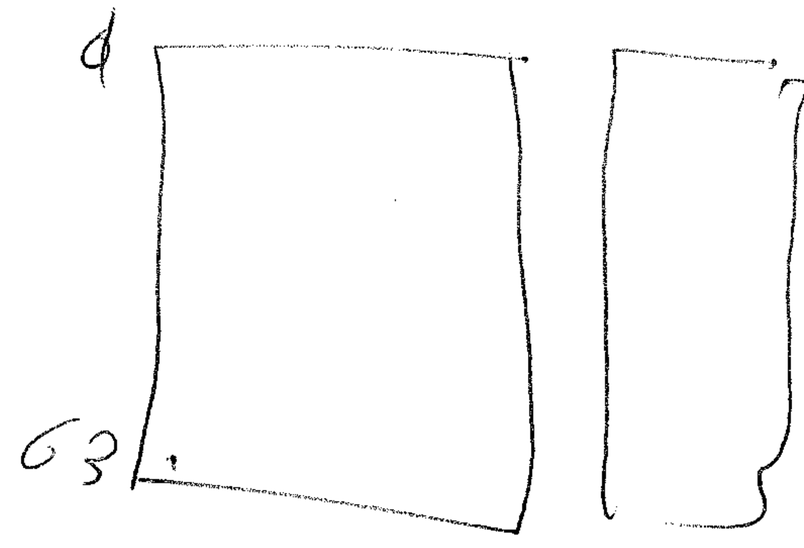
50 %

Q4-ii-Calculate the size of two way set associative TLB that has 128 entry for a 40 bit virtual address and a 32 bit physical address if page size is 16 KB and it uses 4 bits for protection, valid and modify.

4







Tag = 40 − 20 = 20

Tag size = 2 X (20 + 4 bits) * 64

= 128 x 24 = 128 x 3 = 384 B

Data = 2 x 64 x 288 = 36 x 64

= 2304 B

Total = 672 B