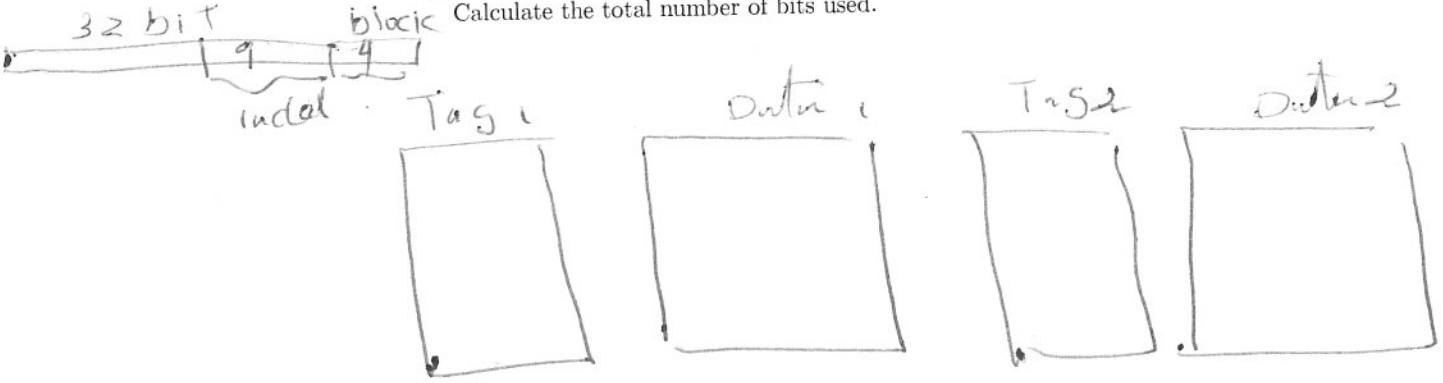
Digital Systems Engineering COE 758
Final Exam, Date: December 10, 2005

Time: 2 hours and 30 Minutes
Answer all the following questions

NAME:_____

1 Q1=10 marks

Assume a two way set associative cache that has a size of 16 KB, a block of 16 B, uses write back and processor address is 32 bit. Calculate the total number of bits used.



# of blocks in each set = $\frac{16KB}{16B \times 2}$ = 512

index $\log_2 512 = 9$ bit

block select = $\log_2 16 = 4$ bit

Tag = 32 − 4 − 9 = 19 bit + 1 dirty bit = 20 bit

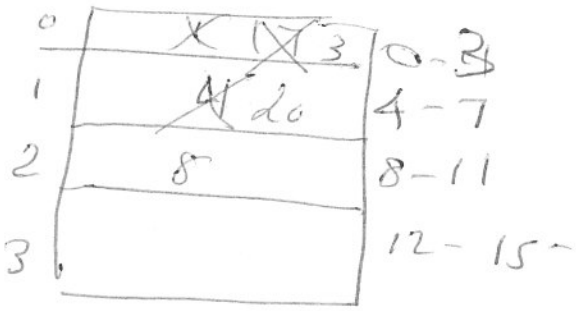
20 bit × 512 × 2 Total Tag = 20 K bit ≈ 2.5 KB

Total size = 16 KB + 2.5 KB = 18.5 KB

2 Q2=10 marks

Assume a direct mapped cache with a size = 16 words, and block is 4 words.
Find the hit rate for the following word address references: 1,4,8,5,20,17,19,3,7

Memory	block	index	
1	0	0	miss
4	1	1	mis
8	2	2	mis
5	1	1	hit
20	5	1	mis
17	4	0	mis
19	4	0	hit
3	0	0	mis
7	1	1	mis



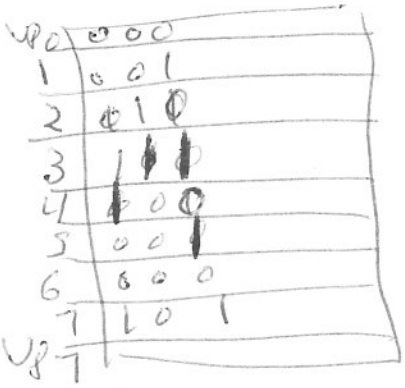
$$\text{hit} = \frac{2}{9}$$

3 Q3=10 marks

Assume a fully associative TLB with two locations. TLB tag has 7,4 and the corresponding data =5,4. Assume that the most significant bit in the data of TLB is used for valid bit. The page table has 8 locations with values =0,1,2,7,4,1,0,5 and the most significant bit is used for valid bit. Page size= 1KB, VM size= 8 KB, Memory size= 4 KB.

Find TLB hit rate and Page hit rate for the following accesses:
3577, 7801, 4327, 900, 2056.

P. Table



1KB

VP# $\frac{3577}{1024} = 3$ TLB Fault, Page hit

VP# $\frac{7801}{7\times1024} = 7$ TLB hit / Page hit

VP $\frac{4327}{1024} = 4$ TLB hit, Page hit

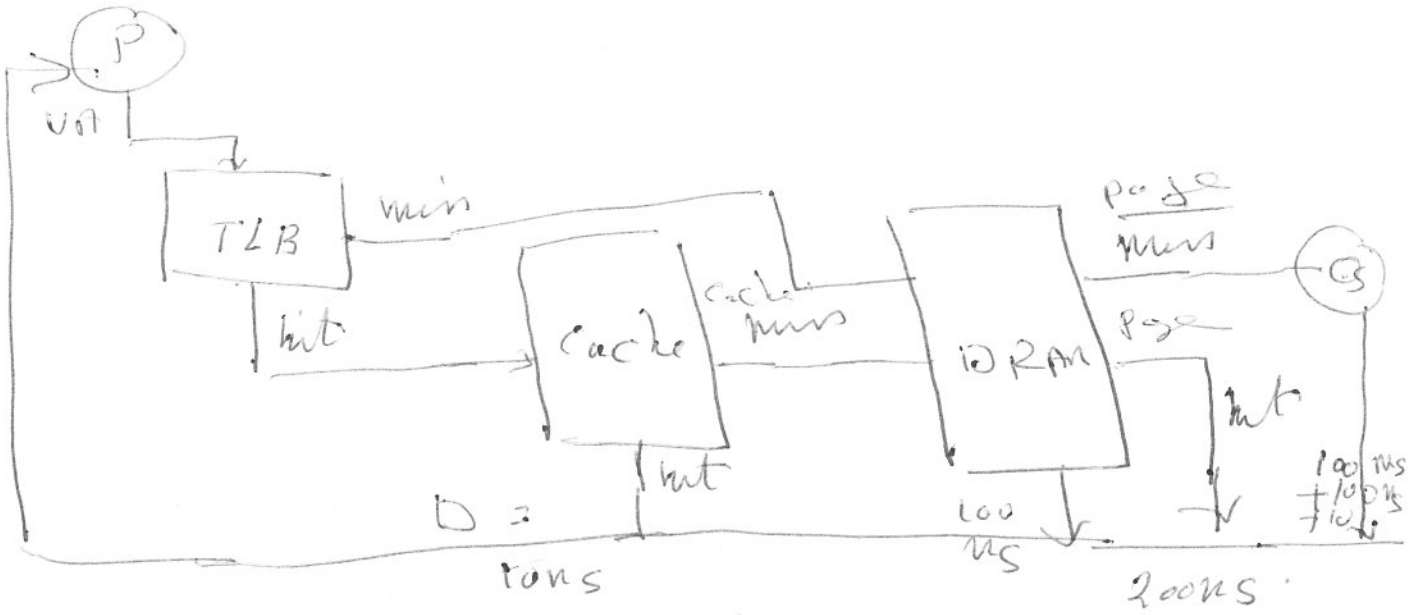
VP $\frac{900}{1024} = 0$ TLB ~~miss~~ / Page miss

VP $\frac{2056}{1024} = 2$ TLB miss / Page miss

TLB hit $= \frac{2}{5}$ Page $= \frac{3}{5}$

4 Q4=10 marks

Draw a block diagram of the overall memory system showing all memory levels from TLB to H.D.. Also show the possible conditions to access each level and the cost of each access if cache latency = 10 ns, memory latency = 100 ns, and H.D. latency = 10 ms.



5 Q5=10 marks

5.1

Explain all steps required for DMA operation

1- Processor Initialize controller with start Address, size of Transfer
2- DMA Controller, Arbitrate For memory BUS, when grant
3- DMA Trans for Data To/From memory with starting Address for size required
4- when finish it interrupts Processor of end of DMA Transfer

5.2

Explain the different methods used to increase bus bandwidth

1- wider Data bus
2- non multiplexed Data/Address
3- block Transfer
4- split Transaction/ Pipelining

5.3

Explain how an Input/Output device transfers data to processor

1- Polling
2- Interrupt
3- DMA

5.4

Explain arbitration and give an example of an arbiter

Multiple devices share one bus, they must arbitrate for it by request.. Arbiter, grant only one Device the use of bus.
1- Example: Daisy chain, simple. Device request to Arbiter has highest priority, one request for All, must be passed through Devices to Arbiter, grant from Arbiter must also be passed through Devices to requested device -

6 Q6=10 marks

Assume a program that uses the following three steps:-
i-Reads 8 KB block of data from hard disk
ii-Spends 50 million cycles for processing the data at 500 MHz clock rate
iii-Writes back the results of 8 KB block to hard disk.
Assume that the disk RPM = 10000, seek time=8 ms, overhead=2 ms, and transfer rate=50 MB/sec.
Find the total time of the program.

T = Read 8KB from H.D
+ processing time
+ write result back of 8KB to H.D

$$\text{Read Time} = 8 + 2 + \frac{1/2}{10{,}000/60} + \frac{8KB}{50MB}$$

$$= 8 + 2 + 3 + .16\ ms = 13.16$$

write same 13.16

$$\text{processing Time} = 50 \times 10^6 \times 2 \times 10^{-9}$$

$$= 100\ ms$$

Total = 126.32 ms

7 Q7=10 marks

Assume a NUMA distributed shared memory multiprocessor system.
Give the outcome of P1 directory state, P2 directory state and Bus operation after executing each of the following sequence:

- P1 reads X1
- P1 writes 10 to X1
- P2 reads X1
- P2 writes 20 to X1
- P1 reads X1