COE758: DIGITAL SYSTEMS ENGINEERING Fall 2018

1 Objectives

COE 758: This course covers the basics of advanced computing systems. The emphasis is in understanding the system architecture around the processor and the different components of modern digital systems.
The course covers Memory hierarchy including Main memory, Cache , Virtual memory and disk technology. It covers the Interfacing of processors and peripherals including Input / Output devices as Video-Output Subsystem. The course gives classification of Buses, bus organization and protocols. The course gives an introduction to systems interconnect and NoC.
The laboratory projects include design of On-Chip Memory controller and Video-signal generator for VGA-monitor.

2 Course Outline

WEEK	LECTURE	LABORATORY
1	**Memory Hierarchy** - Introduction Main Memory: Static RAM	**Lab1: Introduction to** recent FPGA/CPLD technology
2	**Memory Hierarchy** Main Memory: Dynamic RAM (SDRAM, DDR RAM , RDRAM)	**Lab2: Introduction to** FPGA-based development Environment
3	**Memory Hierarchy** Cache memory: Concept and principles of organization	**Lab3: Project 1 (Memory** controller) description and device specification
4	**Memory Hierarchy** Cache memory; Cache Controller's architecture. Multi-level Cache.	**Lab4: Memory Controller;** Design entry (VHDL code)
5	**Memory hierarchy** Virtual memory: Concept and principles of organization	**Lab5: Memory controller:** Simulation and verification
6	**Memory hierarchy** Virtual memory: Interaction between Cache Main memory and Disk in Virtual memory. Disk technology and RAID	**Lab6: Memory controller:** Hardware implementation & real performance analysis.
7	**Interfacing Processor and Peripherals** - IO Devices - Interfacing IO Devices	**Lab7: Demonstration of** Memory controller

WEEK	LECTURE	LABORATORY
8	**Interfacing Processor and Peripherals** - Buses: Concepts and Principles - Midterm Test	**Lab8: Project2: Video-** signal generator: Device specification
9	**Interfacing Processor and Peripherals** -Bus arbitration -Direct Memory Access (DMA)	**Lab9: Video-signal** generator: Design entry (VHDL code)
10	**Multiprocessor System Interconnect** -Introduction -Bus design for single level snooping cache	**Lab10: Video-signal** generator: Simulation and verification
11	**Multiprocessor System Interconnect** -Split-transaction Bus Design	**Lab11: Video-signal** generator: Hardware implementation & real performance analysis
12	**Multiprocessor System Interconnect** -CASE Study: SGI Bus System Design	**Lab12: Integration of** Video-signal generator with SVGA-monitor
13	**Review**	**Lab13: Demonstration of** complete project and final report

3 Course Texts

David Patterson and John Hennessy "Computer Organization & Design The Hardware Software Interface" Morgan Kaufmann Publishers, San Francisco, CA 94104, ISBN 1-55860-428-6

4 Marking Scheme

Total Lab Work = 30%
Midterm = 25%
Final Exam = 45%

All of the required course specific written reports will be assigned not only on their technical or academic merit, but also on the communication skills of the author as exhibited through these reports.

Instructor Name: Dr. Nagi Mekhiel
Office: ENG 446
Telephone: (416) 979-5000 ext 7251
E-mail: nmekhiel@ee.ryerson.ca