Ryerson University
Department of Electrical and Computer Engineering
COE 758 – Digital Systems

Midterm Test **October 29, 2018**

Name: _____ **Student Number:** _____ **Section:** _____

Time limit: 1 hour 50 min Examiners: N. Mekhiel

Notes:
a) Closed book.
b) No calculators.
c) Answer all questions **in the space provided.**

Marking: Each question=10

Q1-Compare the advantages and disadvantages of each of the following choices:- (10)

A-Using address lines for DRAM versus address lines for SRAM

(2) DRAM Address is Multiplexed less number of lines chip packaging small, but needs Latches and slower compared to SRAM

(2) B-Using precharge interleaving versus fast page mode for Multi-bank DRAM

Precharge no Cost good for low order multi-bank interleaving, Fast page needs Computer ad row latch and good for high order interleaving and fasteraccess

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E-Using pages versus segmentation for virtual memory

(2) pages reduces Transfer time less Fragmentation but needs larger page-Table

Q2- A memory system uses **4MX8** DRAM with 2 banks mapped around low order address interleaving and fast page mode. (10)

Find the page hit rate of accessing the following addresses in sequence. The addresses are given in hex.

	row #	bank #	outcome	
-52BC5A	52B	0	miss	(2)
-52AC5A	52A	0	miss	(2)
-52BC3B	52B	1	miss	(2)
-52AD78	52A	0	hit	(2)
52BD5F	52B	1	hit	(2)

hit rate = $\frac{40}{100}$

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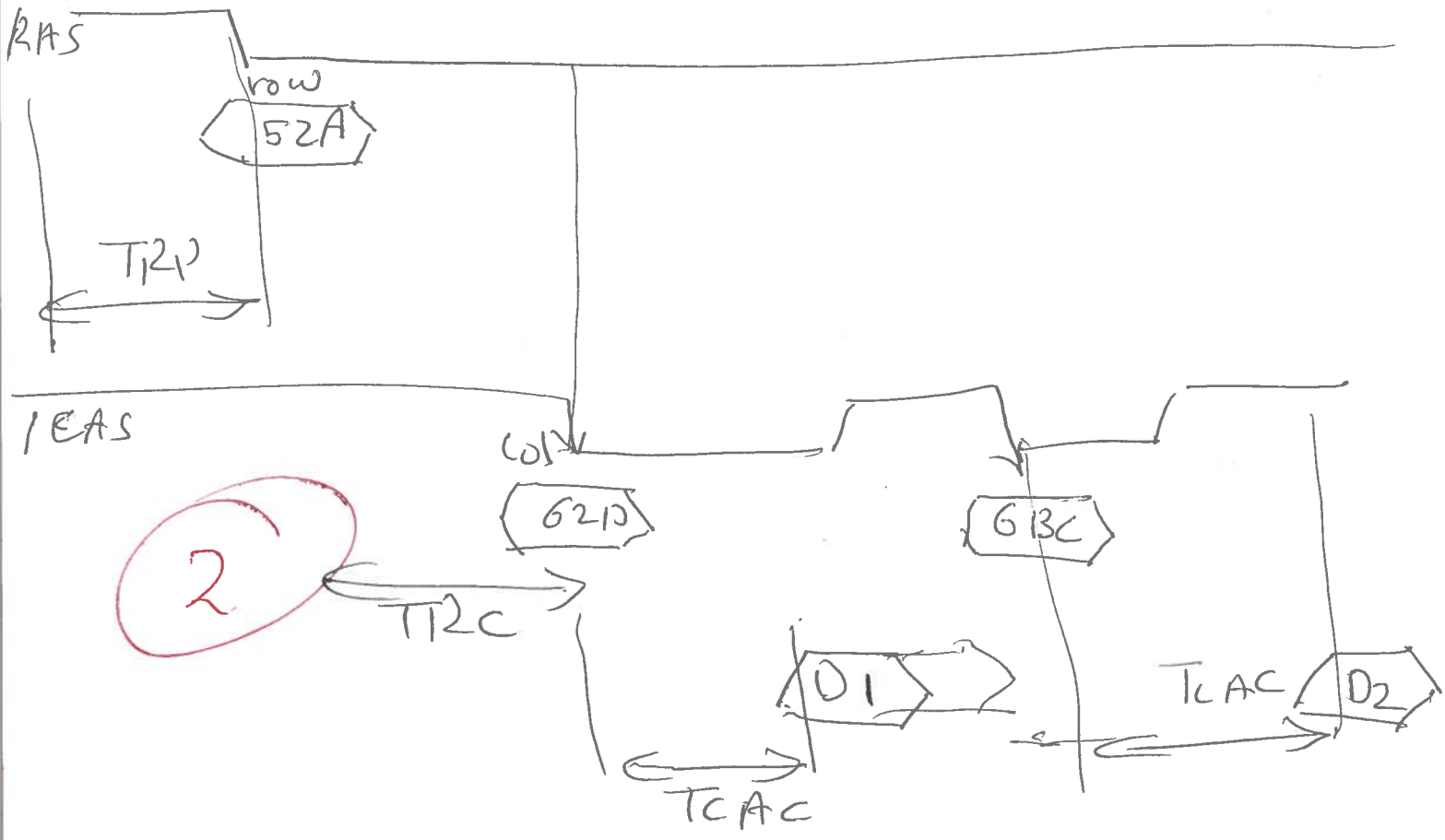
Q3-A-Draw the timing of accessing the above memory system of 52AC5A followed by 52AD78 using fast page mode assuming precharge TRP=4 cycles, TRC=3 Cycles and TCAC= 3 Cycles. Calculate total time in cycles for the two accesses.



$T = TPR + TRC + 2TCAC = 4 + 3 + 6 = 13$ cycles (2)

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Q3-B-Explain the operation for each timing parameter in DRAM:-

2 -TPR

Precharge capacitors in row to Full potential

-

-TRC

2 wait for Row to be decoded and activate row Capacitors

2 -TCAC

wait to decode Column and activate Sense Amp to get data

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(2) C-Using larger cache block versus smaller cache block

Larger block gives better hit rate but increases transfer Time

D-Using two way set associative cache versus direct mapped

Two way set associative better hit rate but needs more comparators and slower

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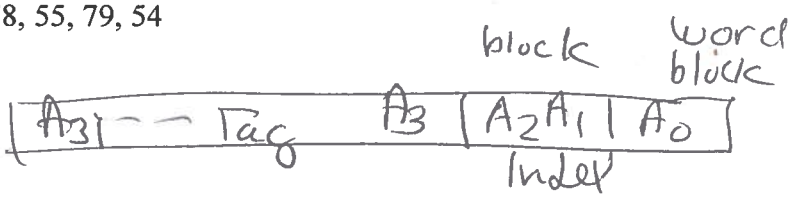
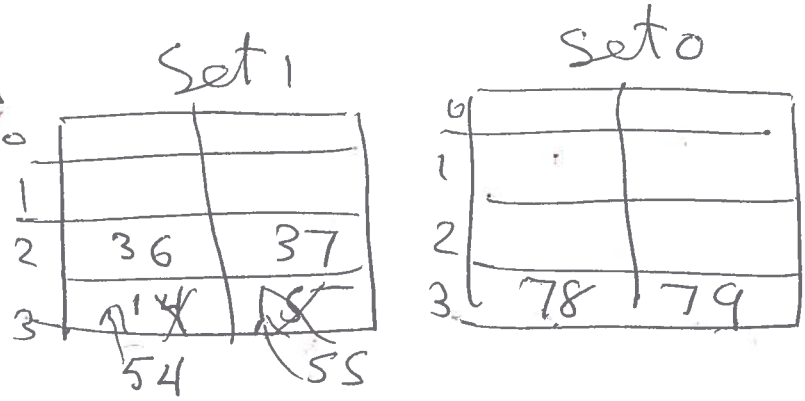
Q4-A- Calculate the hit rate for two way set associative cache of size=16 words assuming block size =2 words and it uses LRU policy for the following sequence of accesses:-

15, 37, 14, 36, 78, 55, 79, 54



index = (A / 2) mod 4



(1) 15 / 2 = 7 mod 4 = 3 miss

(2) 37 / 2 = 18 mod 4 = 2 miss

(3) 14 hit

(4) 36 hit

(5) 78 / 2 = 39 mod 4 = 3 miss

(6) 55 / 2 = 27 mod 4 = 3 miss evict LRU

(7) 79 hit

(8) 54 hit

hit rate = 4/8 = 50%

-1 each mistake

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Q4-B- Calculate average access time for two level cache system assuming number of memory requests =10,000 and 9200 were found in L1 cache, and 600 found in L2 if the following:-

4

L1 access time = 1 ns, L2 access time = 10 ns, and main memory access time = 100 ns.

$$M_1 = \frac{800}{10,000} \times 100 = 8\%$$

$$M_2 = \frac{200}{800} \times 100 = \frac{25}{100} = 25\%$$

$$T_{av} = T_{L1} + M_1 T_{L2} + M_1 M_2 T_M$$

$$= 1 + .08 \times 10 + .08 \times .25 \times 100$$

$$= 3.8 \text{ ns per access}$$

(-1) each mistake

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Q5-A-Assume virtual memory size=16 KB and main memory size= 4 KB and page size=2KB. The content of page table from base=0,2,1,0,3,2,1,0 with most significant bit used as valid bit. Find page hit rate of the following (not in sequence):
507, 1053, 3100, 7500, 6210, 9840

Page Table

	V	
0	0	0
1	1	0
2	0	1
3	0	0
4	1	1
5	1	0
6	0	1
7	0	0

PP

0	VP1, VP5
	VP4

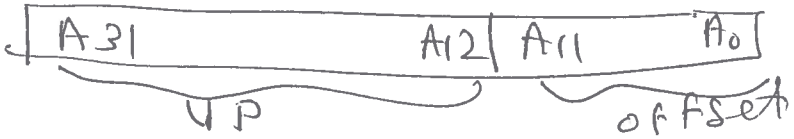
Accss	VP#1	Fault/hit
(1) 507	0	Fault
(1) 1053	0	Fault
(1) 3100	1	hit
(1) 7500	3	Fault
(1) 6210	3	Fault
(1) 9880	4	hit.

page Fault $\frac{3}{6} = 33\%$

P0 0 – 2048
P1 2048 – 4096
P2 4096 – 6144
P3 6144 – 8192
P4 8192 – 10250

(4) Q5-B-Calculate the size of page table for 32 bit virtual address and 24 bit physical address if page size is 4KB and it uses 2 bits for valid and protection

page offset



offset = $\log_2 4K = 12$
VP address = $32 - 12 = 20$
# of pages = 2^{20}
physical page address = $24 - 12 = 12$
size of Page Table = $2^{20} \times (12+2) = 1.66MB$

(2) (2)