Digital Systems Engineering COE758
Final Exam, Date: Dec 3, 2013

Time: 2 hours and 30 Minutes
Answer all the following questions
Calculators Allowed

Student Name _____

Q1 – =10 marks

Explain the reasons for the following:-

A-Set Associativity Improves cache Hit rate

Reduces Conflict Misses

B-Using LRU Improves Cache Hit rate

Temporal locality

C-Using separate data and instruction cache has worse hit rate compared to unified cache, but gives better performance

eliminates a pipeline hazard when load & Fetch at same cycle

D-Write Allocate gives better performance than No Write Allocate

When Data is Read there is a chance that it will be used soon and WA will have it in cache.

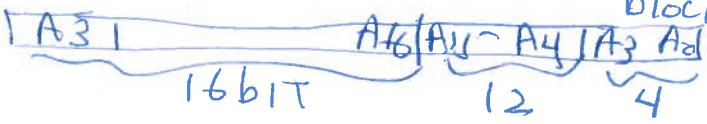
Q2- =12 marks

A-Calculate the total size of a 128 KB, two way set associative cache, if block size = 16 B, uses 1 dirty bit and assume processor address= 32 bit.

number of blocks = $\frac{128KB}{16B}$ = 8K

each set 4K entries

index Address = $\log_2 4K$ = 12 bits



Tag size = 32 − 12 − 4 = 16 + 1 dirty bit

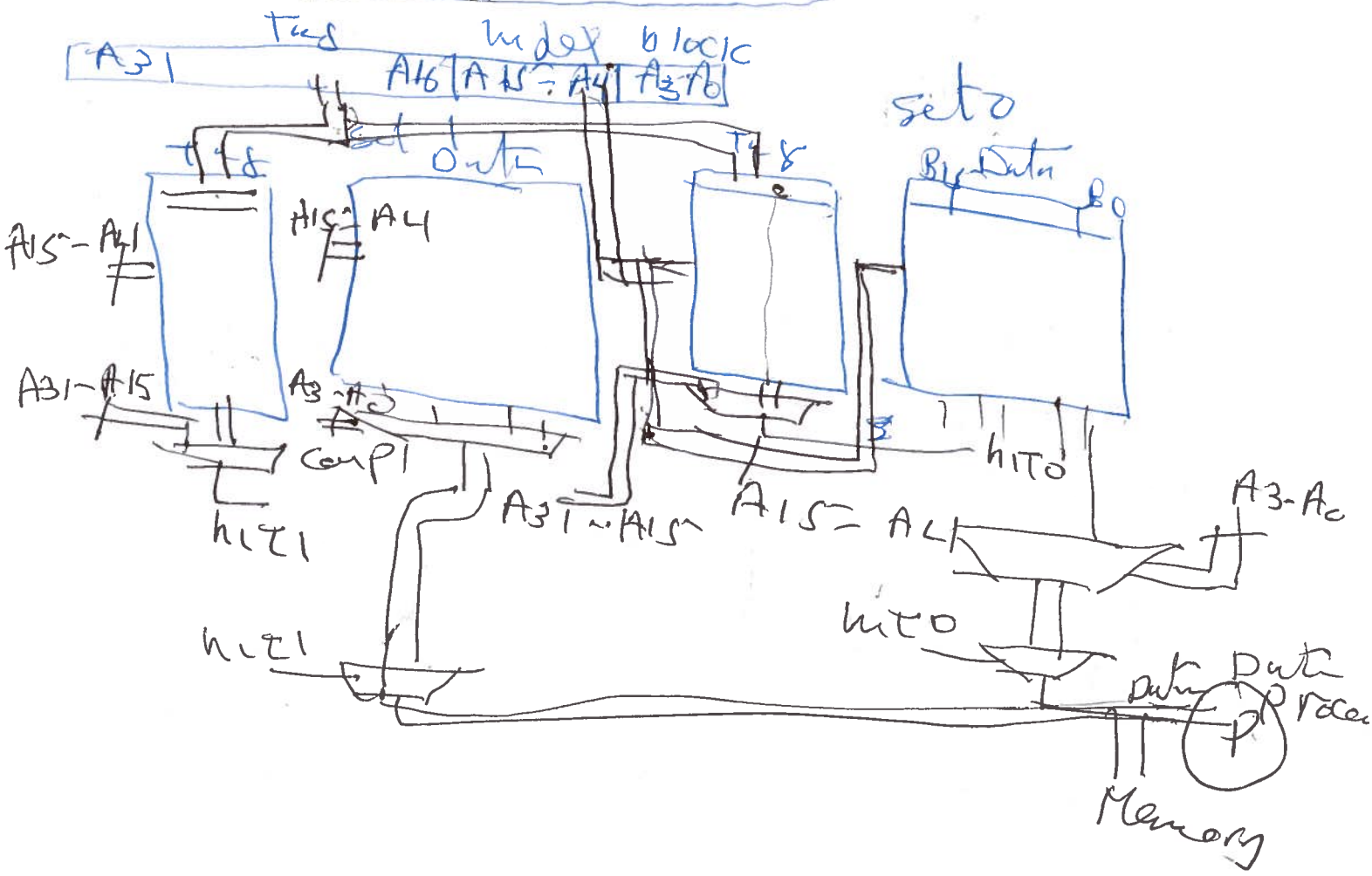
Size of Tags = 8K × 17 bit ≈ 16KB

Total size = Data + Tags = 128KB + 16KB = 144KB

Q2-B- In the above cache, calculate the tag of an access to address 005E7000 HEX.

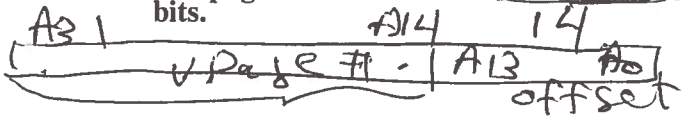
Tag = 005E = 16×5 + 14 = 94 decimal

Q2-C- Draw the block diagram of the above cache showing tags, data cache and buses connecting processor data and address to cache.



Q3- =12 Marks

A-Calculate the size of page table for 1 MB physical memory if page size= 16 KB, and page table uses 1 extra bit for valid. Assume processor Virtual address = 32 bits.



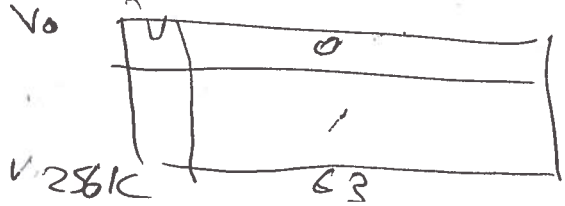
offset = $\log_2$ 16KB = 14 bit

# of physical pages = $\frac{1\,MB}{16\,KB}$ = 64 pages

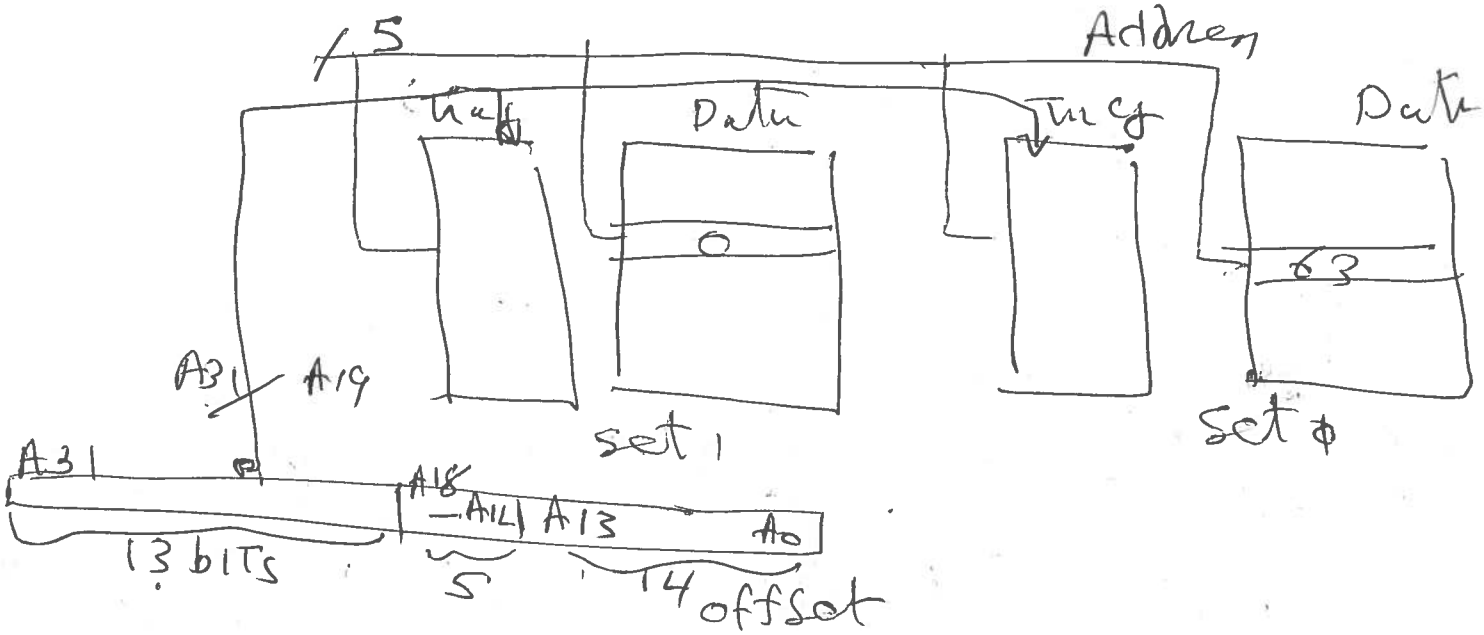
# of bits $\log_2 64$ = 6 bits

Size of Page Table = # of V. Pages X number of bits to point to a physical page + 1 valid

= 2^{18} X 7 bits = 256KB



B- Calculate the size of TLB, if the above system uses two way set associative TLB with 32 enteries for each set and one bit for valid.

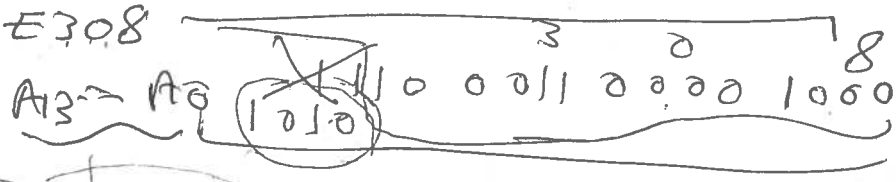


Data = 64 X 7 bits = 64 B

Tag = 64 X 13 = 64 X 2.5 B = 128+32 = 160 B

C-In the above system, translate the virtual address 0A00E308 to physical address, assuming this Virtual page maps to physical page 10.

VA = 0A00E308

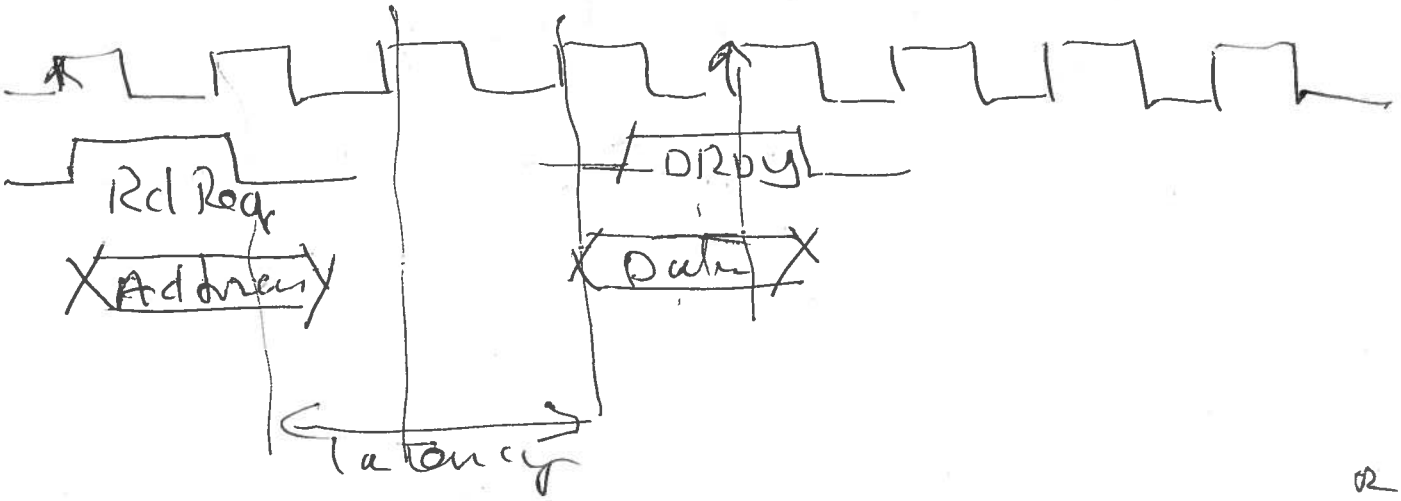


10 1010 308

hex = 2A308.

Q4- = 10 Marks

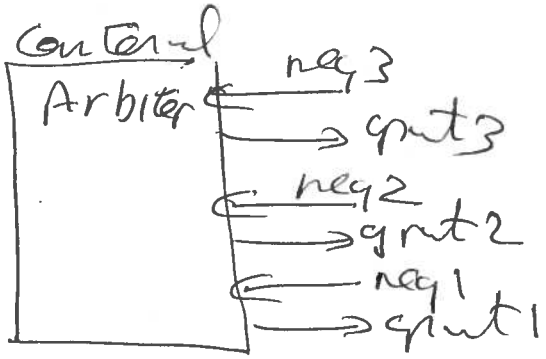
A-Draw the timing diagram of Synchronous bus Read assuming device latency = 2 cycles, one cycle to send address and one cycle to send data.



OR

B-Explain by giving a block diagram the operation of a Central Arbiter and how a grant is generated for each device.

- Each Device Request The bus
- Central Arbiter only respond by giving a grant to the highest priority



$grnt3 = req3$

$grnt2 = \overline{req3} * req2$

$grnt1 = \overline{req3} \cdot \overline{req2} \cdot req1$

C- What are the parameters that affect the transfer time of a block from hard disk

T= seek Time + RPM + Bw of Transfer

Q5=10 Marks

Q5-A- Explain how and why a DMA is used to transfer data from a device

how: 1- Processor Initialize DMA Controller with Address + number of bytes To Transfer
2- DMA Takes Control, Arbitrate For memory and start Transfer Data To/from Address until it finishes the size of transfer
3- it will interrupt the processor

why: - it Saves processor Time as it will NOT be involve in Transfer

Q5-B-Why DMA use might cause problem to cache system

Data will be different from the Data cache (not coherent)

Q5-C-Assume a 1 GHz processor that uses DMA to transfer 16 KB from H.D to Memory. The setup time of DMA transfer = 1000 cycles and the interrupt requires 400 cycles. The transfer rate is 2 MB/sec.

Calculate the fraction of processor time consumed in the transfer

Each Transfer processor Time
$= 1000 + 400 = 1400$ cycles

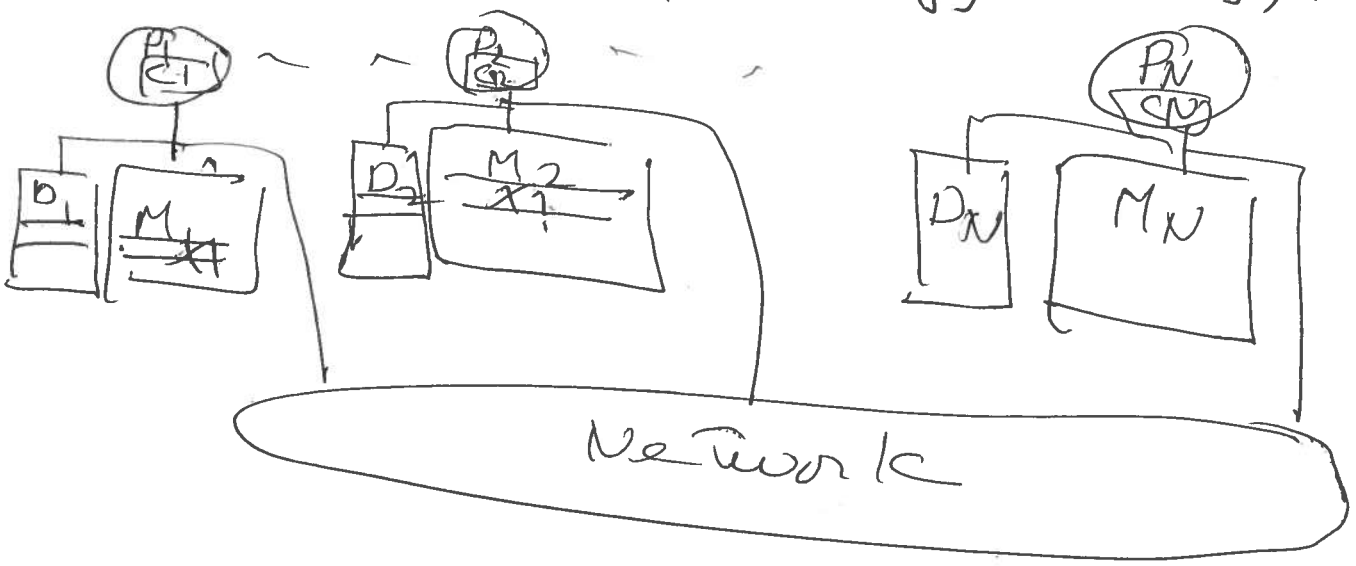
Transfers per second $= \frac{2\ MB}{16\ KB} = 128$

time $= 1400 \times 128 \times 100 \times 10^{-9}$
$= .0179\ \%$

Q6=12 Marks

Q6-A-List the main components used in distributed shared memory multiprocessor system and draw a block diagram.

- Processor, cache, Memory, Directory, Network



Q6-B- Assume a shared memory distributed multiprocessor system and X1 in P1 memory, and X2 is in P2 memory. Give the directory state , bus operation and cache state for the following:-

1. -P2 reads X1
2. -P1 reads X2
3. -P1 Writes to X1
4. -P2 reads X1

1. Bus ~~Address~~ X1, Read — P2 C2 = X1 shared
   P1 D1 label X1 shared (P1, P2)
2. bus has address X2 Read
   P1 C1 has X2 label it shared
   P2 D2 has X2 shared P1, P2

(3) P_1 writes to X_1 ; Bus has Address X_1, INV
C_2 in P_2 mark X_1 as INV

P_1 = Cache has X_1 as EXCLUSIVE
D_1 = has X_1 as EXCLUSIVE

(4) P_2 needs X_1 ; Bus Address X_1, Read
P_2 will have X_1 in C_2 labeled shared

P_1 C_1 has X_1 as Shared
D_1 in P_1 has X_1 as Shared between P_1, P_2