Digital Systems Engineering COE 758 Midterm 2015

Time: 1 hour and 50 Minutes Each question=10 marks Answer all the following questions

1 Q1

-Briefly compare the advantages and disadvantages of the following:-
1-DRAM versus SRAM
2-Open page policy (Fast page mode) versus closed page with (autoprecharge)
3-direct mapped versus two way set associative cache
4-Using larger cache Block size
5-Virtual memory using Paging versus Segmentation

1- DRAM has large capacity, small size
SRAM has high speed

2- could improve performance if high hit rate,
cost a comparator,
closed page simple, improve performance
if no bank conflicts

3- Direct mapped is fast, simple to implement
two way set associate has high hit rate

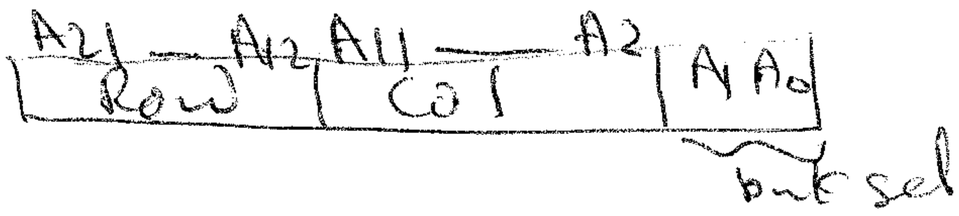
4- Large cache block has higher hit rate
but increases time for

5- Paging has low time for time on fault,
segmentation has small segm. Table
better protection

2 Q2-i

-A memory system uses 4-Banks with open page and low order address interleaving implemented with 1MX8 DRAM modules.

Find the page hit rate for the following sequence of ~~the following~~ addresses: 1200, 1201, 1600, 2401, 6501 and 7501 (find bank, row of each access)

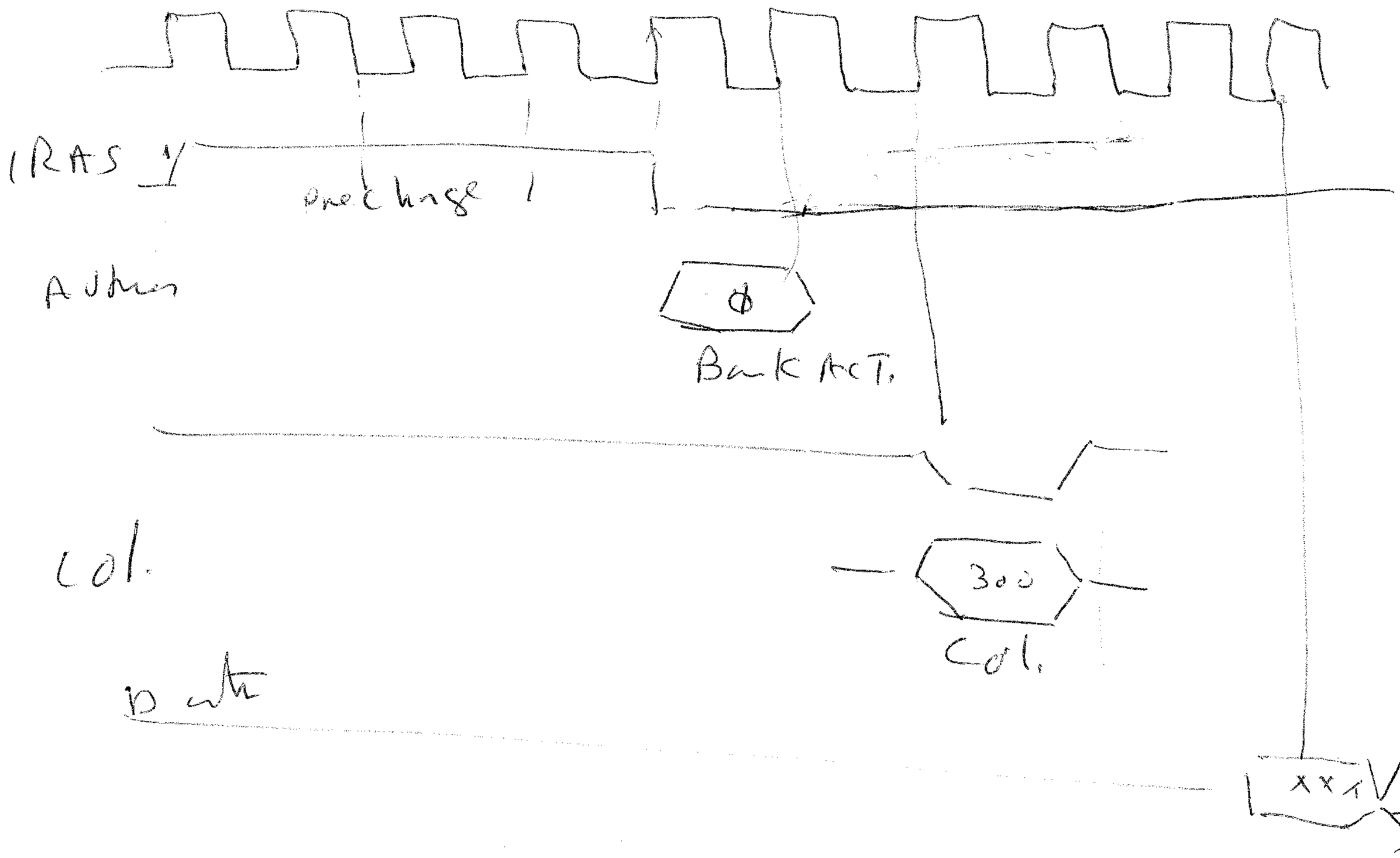


Accen	bank #	row #	
1200	~~bank~~ = 0	= 0	miss
1201	= 1	= 0	miss
1600	= 0	= 0	hit
2401	= 1	= 0	hit
6501	= 1	= 1	miss
7501	= 1	= 1	hit

50 %

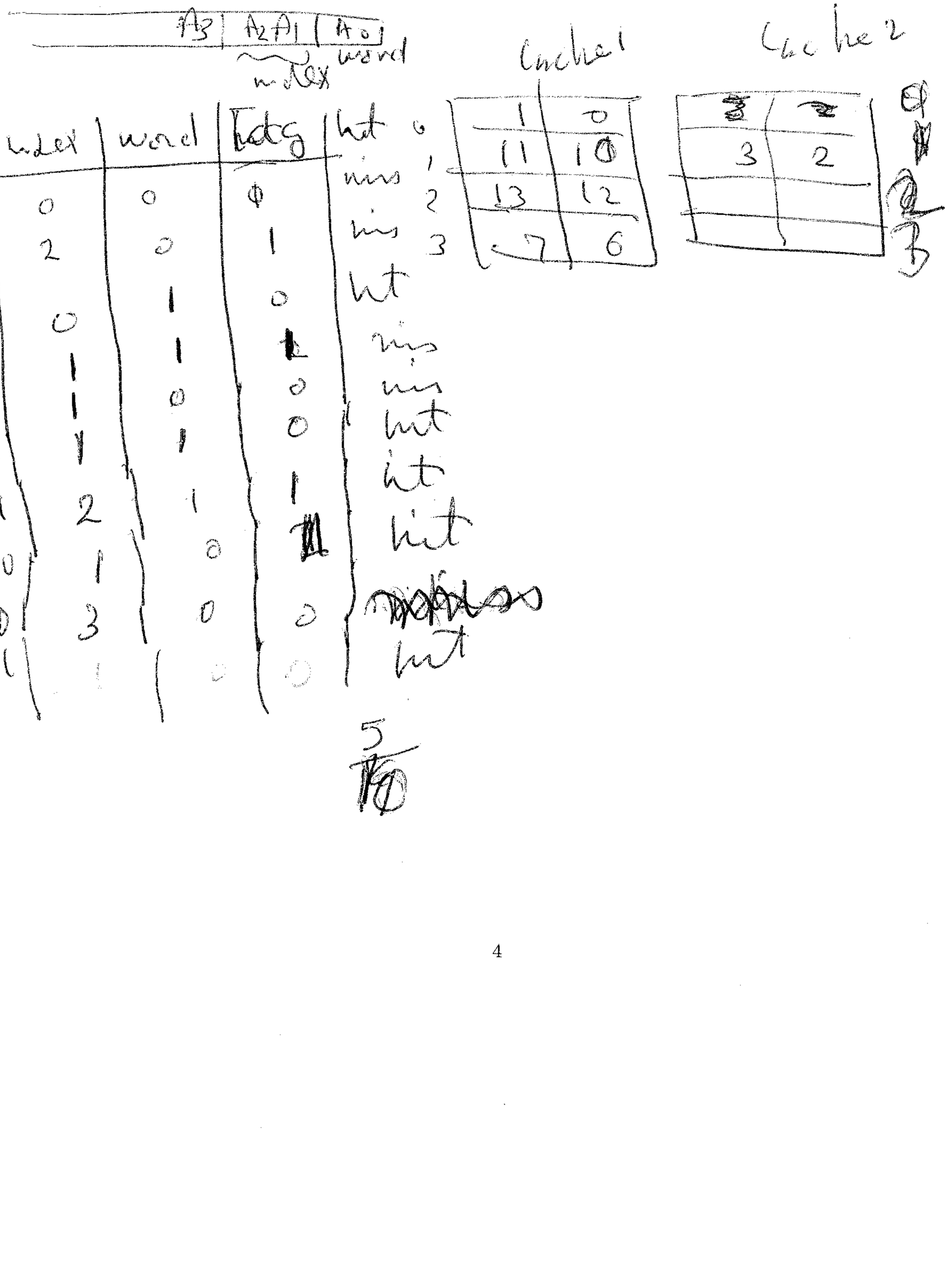
2.1 Q2-ii

- Draw the timing for SDRAM Read operation of location 1200 of above memory assuming: a page miss, precharge time = 3 cycles, bank activation=2 cycles, CAS delay=2 cycles and burst length=8.



3 Q3-i

-A Cache system uses two-way set associative organization with LRU policy. The total size of cache = 16 bytes and the block size = 2 bytes. For the following sequence of accesses, find the hit rate: 0, 12, 1, 11, 2, 3, 13, 10, 6,3



3.1 Q3- ii

-Calculate the average access time of a memory system that uses a direct mapped cache with block size=64 Byte, speed= 1 ns, miss rate= 2and bus width= 64 bit. SDRAM precharge= 2 cycles, bank activation = 2 cycles, CAS latency= 2 cycles. Assume that each cache miss is a page miss access with burst, and SDRAM and bus speed = 200 MHz.

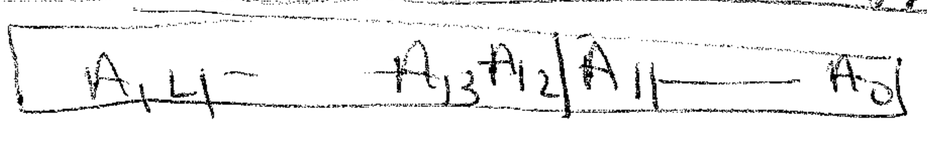
$= 1 + M_1 * T_M$

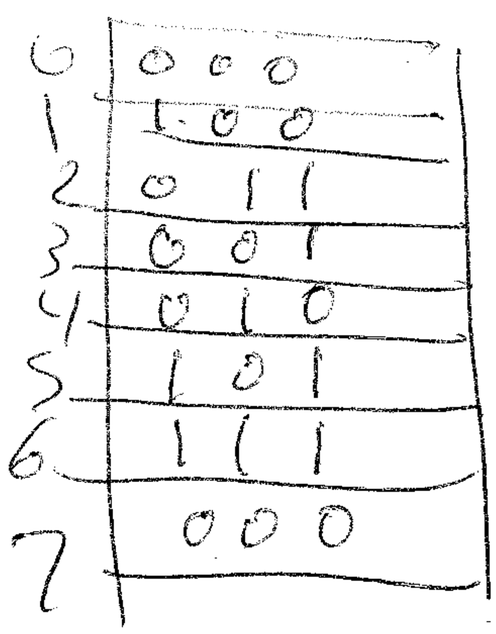
$= 1 + .02 \times ((6+8) \times 5)$

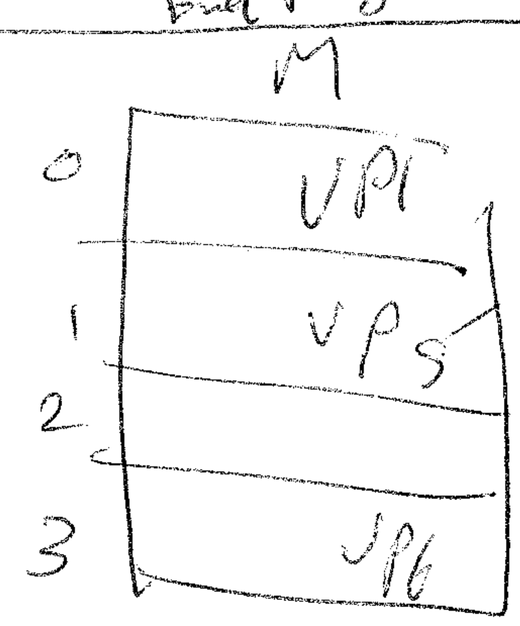
$= 1 + 1.4 = 2.4$ ns

4 Q4-i

-A 32 KByte V.M. space, if main memory size = 16 KByte, page size= 4KByte and the content of page table starting from base is 0, 4, 3, 1, 2, 5, 7, 0 and MSB is used as valid bit. Find 1056, 3567, 4470, 5857, 21567, 25068





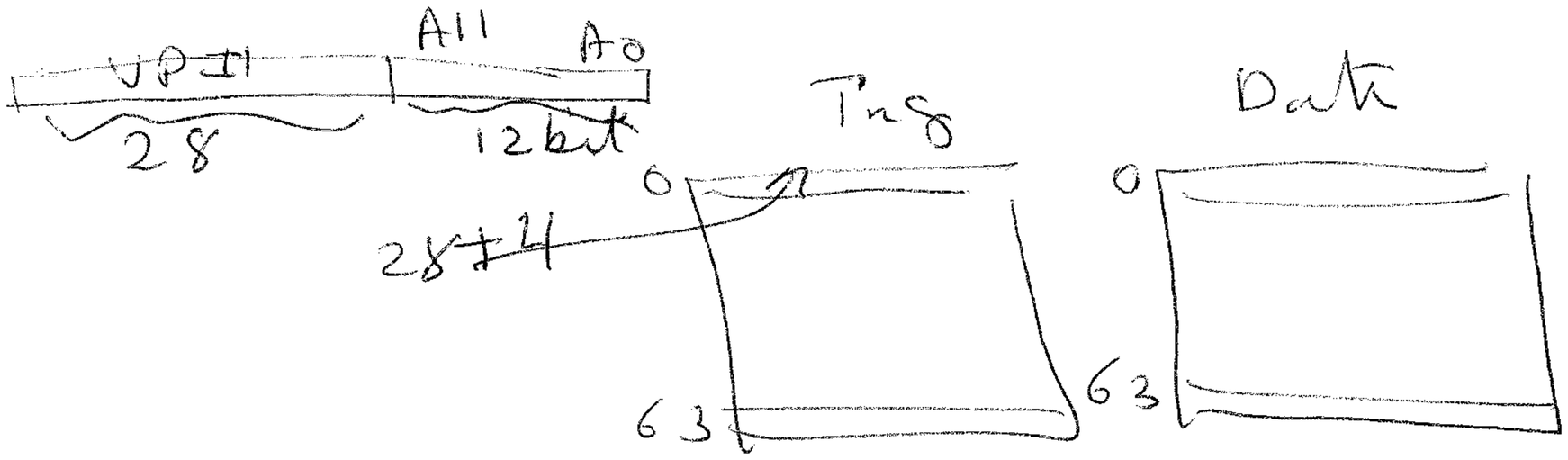


Accen	VP#	hit/fail
1056	0	miss
3567	0	miss
4470	1	hit
5857	1	hit
21,567	5	hit
25,068	6	hit

0 — 4K	0
4K - 8K	1
8 - 12	2
12 - 16	3
16 - 20	4
20 - 24	5
24 - 28	6

4.1 Q4-ii

-Calculate the size of fully associative TLB that has 64 entry for a 40 bit virtual address and a 32 bit physical address if page size is 4 KB and it uses 4 bits for protection, valid and modify.



Tag = (28+4) × 64

Data = (32-12) × 64

Total = 64 × 52 bits

= 416 byte