BME 328 Lab 4 – Adder Subtractor Unit

15 Marks (2 weeks)
Due Date: Week 8

1. Objectives

- To design and build a 4-bit Adder/Subtractor unit (ASU) using an Altera CPLD chip.
- To design an Adder/Subtractor unit that multiplexes add and subtract operations with a common Cin input.
- To implement the 4-bit ASU using VHDL code.
- To design a Combinational Circuit that takes the decoded output of the ASU as input. This Combinational Circuit will have the design logic to output individual digits of the student identification number of the student performing the laboratory work.

2. Pre-Lab Preparation

1. Modify the VHDL code from Figure 5.28 (see course text) to implement the ASU represented in Figure 5.13 (see course textbook). Create a file *ASU.vhd* to accomplish this task. Note: change **ieee.std_logic_signed.all** to **ieee.std_logic_unsigned.all**.
2. Minimize the logic expressions for a 4-bit representation L3, L2, L1, and L0 of your student identification number. Hint: Fill out the truth table below with a 4-bit representation of your student identification number. Then generate the minimized logic expressions for L3, L2, L1, and L0 using K-Maps.
3. Create a new VHDL file *C.vhd* to implement the minimized logic expressions for the L3, L2, L1 and L0 by converting each of the resulting expressions to VHDL code. The Combinatorial Circuit takes the coded output the ASU as input.
4. Using the Functional Simulator (waveforms), verify the circuit described by the VHDL file obtained in step 3. By setting values for X3, X2, X1, X0, Y3, Y2, Y1, Y0 and Cin, observe the following signals: S3, S2, S1, S0and Cout.

ASU Sum Output	**First 8 Digits of Student ID**
S_3 S_2 S_1 S_0	**L_3 L_2 L_1 L_0**
0 0 0 0	
0 0 0 1	
0 0 1 0	
0 0 1 1	
0 1 0 0	
0 1 0 1	
0 1 1 0	
0 1 1 1	
1 0 0 0	
1 0 0 1	
1 0 1 0	
1 0 1 1	
1 1 0 0	
1 1 0 1	
1 1 1 0	
1 1 1 1	

3. Laboratory Work

The procedure is divided into 2 parts:

Part A:

1. This part must be completed during week 1 of this lab experiment.
2. Compile your modified 4-bit Adder/Subtractor unit (**ASU**) file *ASU.vhd* and create a symbol file *ASU.bsf*.
3. Test your design and show your schematics, VHDL codes, and simulation results to your lab instructor. Note: the maximum number of the ASU output S should be 7.

Part B:

1. This part must be completed during week 2 of this lab experiment.
2. Compile your Combinatorial Unit *C.vhd* and create a symbol file *C.bsf*.
3. Start a new project CombinedASU1. Create a block schematic file *CombinedASU1.bdf* as shown in Figure 1 using the *ASU.bsf* and the *C.bsf* symbols that you created earlier.
4. Test your design and show your schematics, VHDL codes, and simulation results to your instructor.

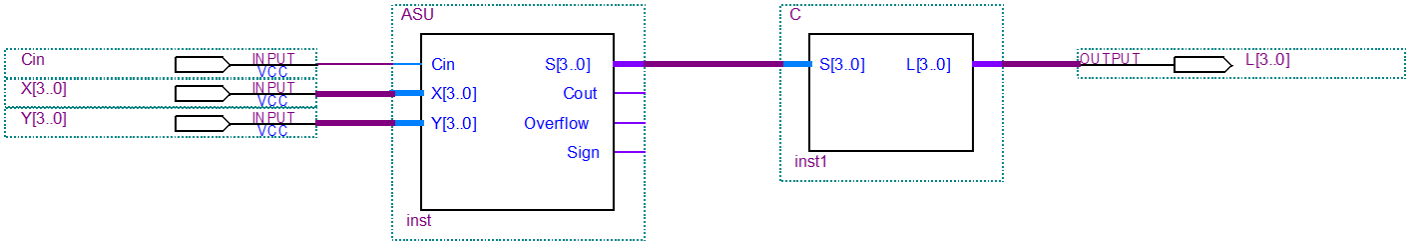

Figure 1: Block Diagram for Part B implementation