LAB 2 TUTORIAL

FUNCTION IMPLEMENTATION AND MINIMIZATION

OVERVIEW

In this tutorial we will build on the circuit implemented in Lab 1 to:

1. Design, build and test a logic function F1 using the Karnaugh map method. We are required to use only NAND gates (4012BP_5V components) and inverters (4009BCP_5V components).

   F1 = (2, 7, 9, 12, 13, 14, 15).

2. The inputs to F1 are the outputs of the counter from the Lab1 circuit Q0, Q1, Q2, Q3.
3. We are required to use an LED with a resistor in series to show the output F1 for all conditions. (i.e. The net F1 should be 1 for values of Q3, Q2, Q1, Q0 corresponding to 2, 7, 9, 12, 13, 14, and 15; and 0 otherwise.

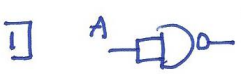
PRE-LAB

① Truth table for 2-input NAND.

$Y = \overline{AB}$

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

② Inverter using 2-input NAND.

1] 

A	Y
0	$\overline{0.0} = \overline{0} = 1 = \overline{A}$
1	$\overline{1.1} = \overline{1} = 0 = \overline{A}$

$Y = \overline{A}$

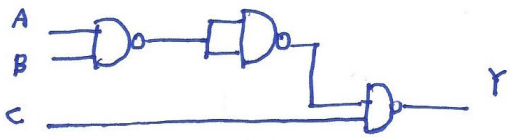
2] 

A	Y
0	$\overline{1.0} = \overline{0} = 1 = \overline{A}$
1	$\overline{1.1} = \overline{1} = 0 = \overline{A}$

$Y = \overline{A}$.

③ 3-input NAND using 2-input NANDS.

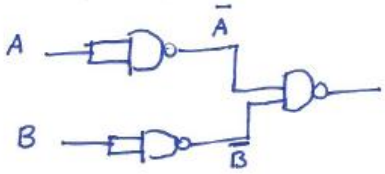
$Y = \overline{ABC} = \overline{(AB)C} = \underbrace{\underbrace{(AB)}_{\text{not(NAND)}}C}_{\text{NAND}}$.



④ 2-input OR using 2-input NANDs.

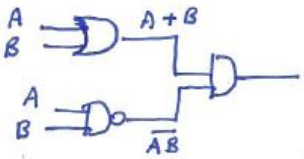
$Y = A + B$.

$\bar{\bar{Y}} = Y = \overline{\overline{A+B}} \xrightarrow{\text{De Morgan}} Y = \underbrace{\overline{\bar{A} \cdot \bar{B}}}_{\text{NAND}}$.



⑤ $Z = f(A, B) = (A + B)\,\overline{AB}$

Using one 2-input OR, one 2-input AND, and one 2-input NAND:



ⓐ Using only NANDs.

$Z = (A+B)\,\overline{AB}$.

$\bar{\bar{Z}} = Z = \overline{\overline{(A+B)\,\overline{AB}}} = \overline{\overline{(A+B)} + \overline{\overline{AB}}}$

$= \overline{(\overline{A+B}) + AB} = \overline{\bar{A} \cdot \bar{B} + AB}$

$= (A+B) \cdot (\bar{A} + \bar{B}) = \overset{\nearrow 0}{A\bar{A}} + A\bar{B} + B\bar{A} + \overset{\nearrow 0}{B\bar{B}}$

$= A\bar{B} + B\bar{A}$.

From Q.4 $\quad \overline{C + D} = \bar{C} \cdot \bar{D}$

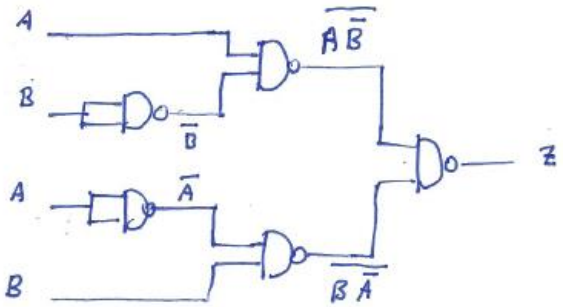
$\therefore Z = \overline{A\bar{B}} \cdot \overline{B\bar{A}}$

⑤ ⓐ Continued.

$$Z = \overline{A\bar{B}} \cdot \overline{B\bar{A}}$$

NAND NAND

NAND.



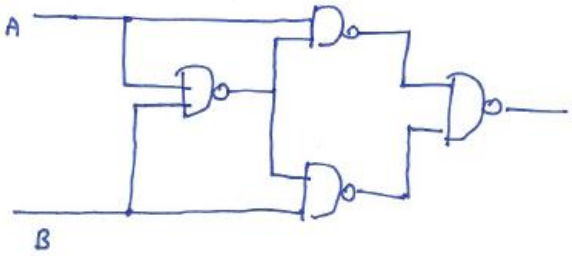
ⓑ Truth table

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

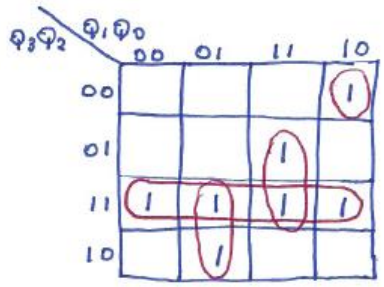
$Y = A\bar{B} + \bar{A}B = A \text{ xor } B$

↳ XOR Gate.

ⓒ $Z = A\bar{B} + \bar{A}B$ → Sum of Products.



⑧ k-Map.



Simplified Logic Equation:

$$F_1 = Q_3Q_2 + Q_3\bar{Q}_1Q_0 + Q_2Q_1Q_0 + \bar{Q}_3\bar{Q}_2Q_1\bar{Q}_0$$

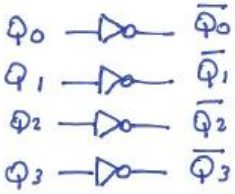
⑨ Convert to NAND (We can only use 4-input NANDs in this lab) and inverters

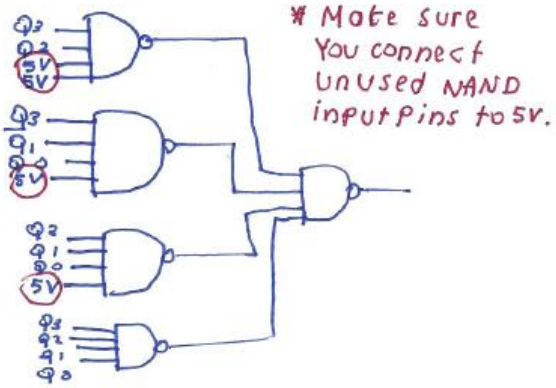
$$F_1 = \bar{\bar{F}}_1 = \overline{Q_3Q_2 + Q_3\bar{Q}_1Q_0 + Q_2Q_1Q_0 + \bar{Q}_3\bar{Q}_2Q_1\bar{Q}_0}$$

$$= \overline{\overline{Q_3Q_2} \cdot \overline{Q_3\bar{Q}_1Q_0} \cdot \overline{Q_2Q_1Q_0} \cdot \overline{\bar{Q}_3\bar{Q}_2Q_1\bar{Q}_0}}$$

NAND NAND NAND NAND

NAND.

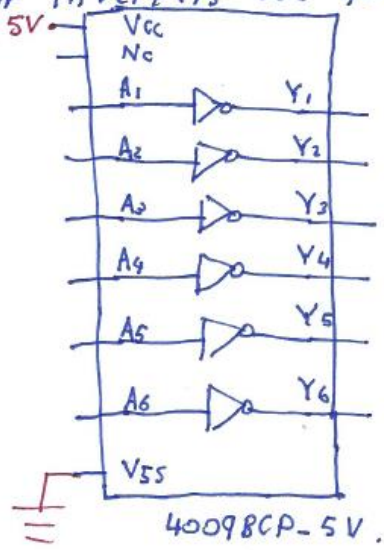




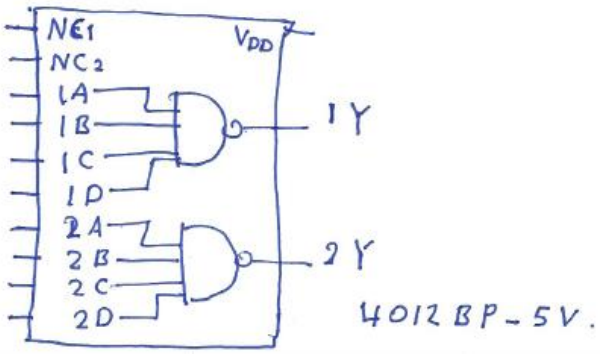
Additional Information:

Use the following Components to Implement in NI Multisim 14.2.

① For Inverters Use 4009BCP_5V.



② For NAND Gates Use 4012BP_5V.



PROCEDURE

1. Schematic Design

Please follow the following instructions to construct the circuit shown in Figure 1:

1. Create a new folder “Lab2” in your “BME328” folder.
2. Open NI Multisim 14.2.
3. From Multisim open your lab 1 design “Lab1.ms14”.
4. Save a copy of “Lab1.ms14” as “Lab2.ms14” in your “Lab2” folder.
5. Modify “Lab2.ms14” as illustrated in Figure 1.

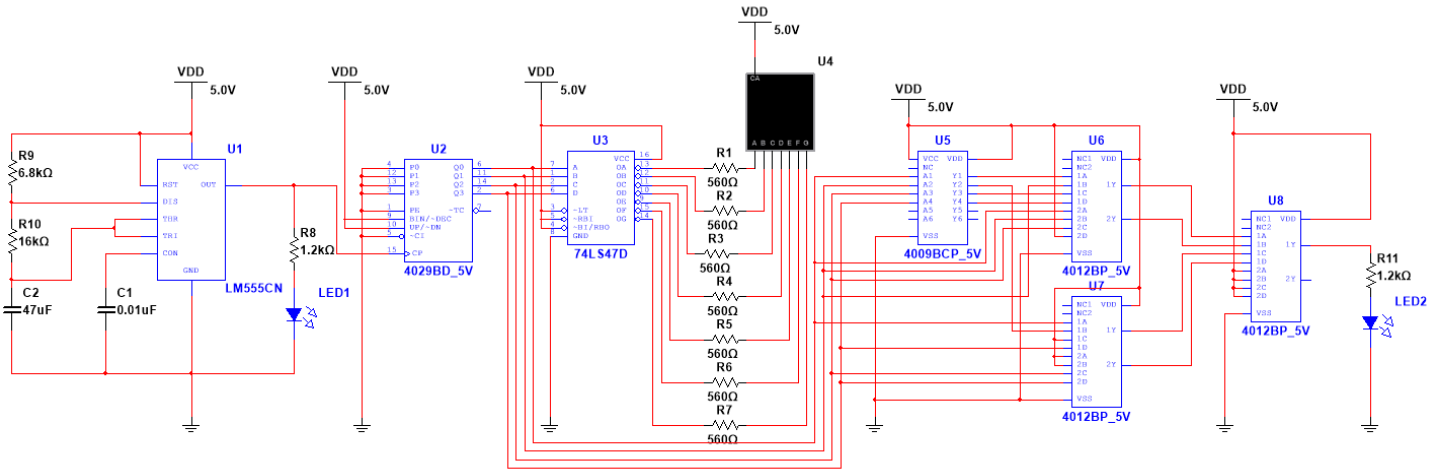


Figure 1

2. Simulations

Before we simulate, we need to label the nets that we wish to simulate. To label a net:

1. Double click on each of the wires highlighted in Figure 2.
2. Then change the “Preferred net name” field as illustrated in Figure 4 (i.e Vout555, etc…)

Save your design.

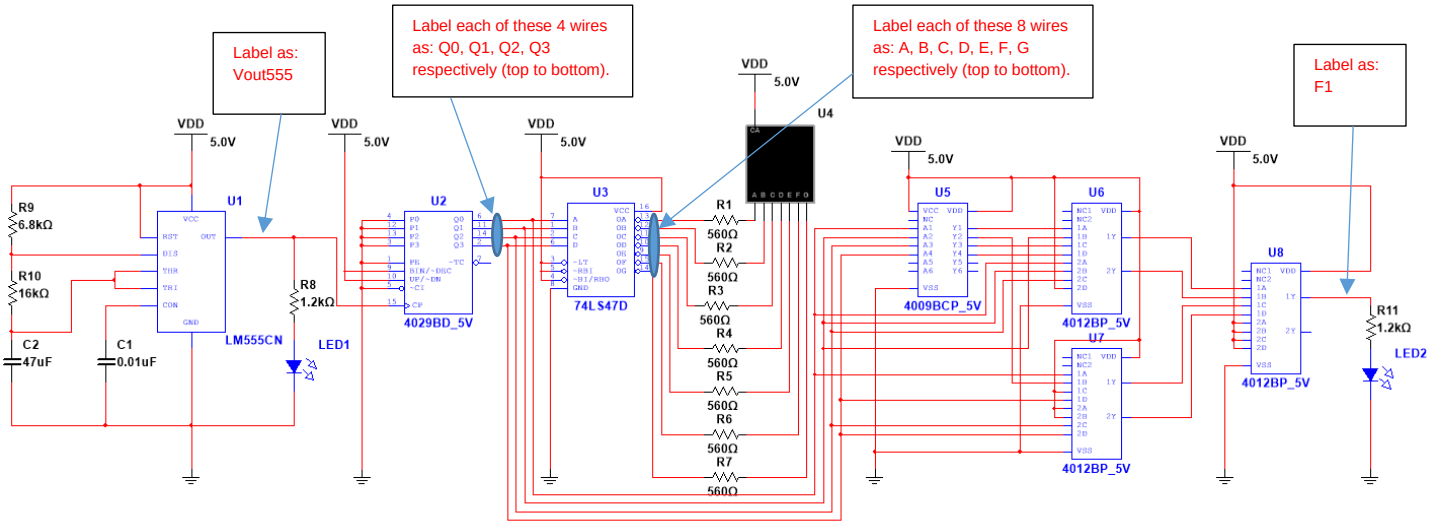


Figure 2

To simulate the design:

1. Click on “Simulate” located at the top left of your Multisim window.
2. Then click on “Analyses and Simulation.”
3. Follow steps 1 to 7 outlined in Figure 3 and Figure 4.
4. Compare your results to Figure 5.

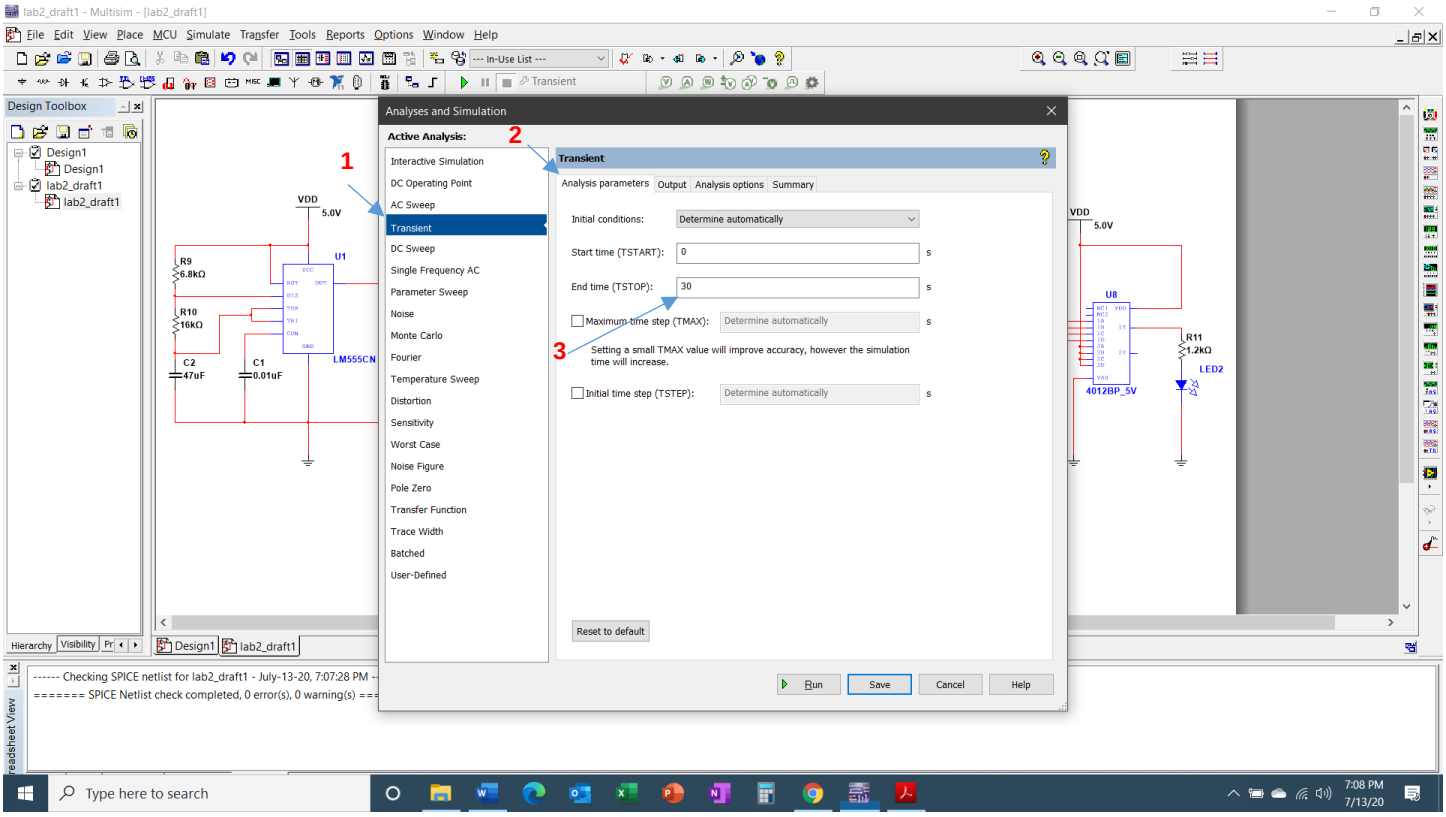


Figure 3

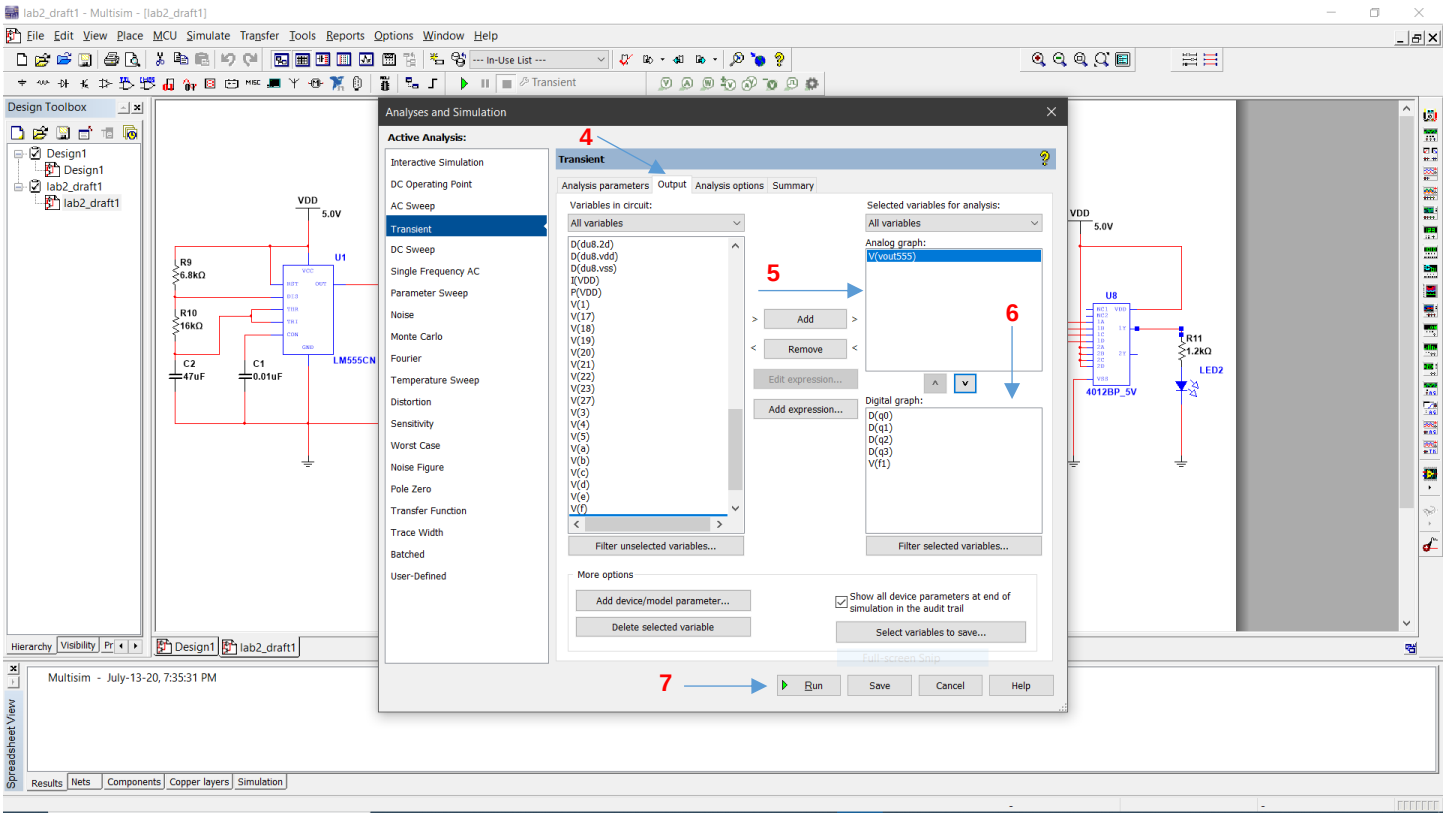

lab2_draft1 - Multisim - [lab2_draft1]
File Edit View Place MCU Simulate Transfer Tools Reports Options Window Help
Design Toolbox
Design1
lab2_draft1
Analyses and Simulation
Active Analysis:
Interactive Simulation
DC Operating Point
AC Sweep
Transient
DC Sweep
Single Frequency AC
Parameter Sweep
Noise
Monte Carlo
Fourier
Temperature Sweep
Distortion
Sensitivity
Worst Case
Noise Figure
Pole Zero
Transfer Function
Trace Width
Batched
User-Defined
4
Transient
Analysis parameters
Output
Analysis options
Summary
Variables in circuit:
All variables
D(du8.2d)
D(du8.vdd)
D(du8.vss)
I(VDD)
P(VDD)
V(1)
V(17)
V(18)
V(19)
V(20)
V(21)
V(22)
V(23)
V(27)
V(3)
V(4)
V(5)
V(a)
V(b)
V(c)
V(d)
V(e)
V(f)
Filter unselected variables...
5
Add
Remove
Edit expression...
Add expression...
Selected variables for analysis:
All variables
Analog graph:
V(vout555)
6
Digital graph:
D(q0)
D(q1)
D(q2)
D(q3)
V(f1)
Filter selected variables...
More options
Add device/model parameter...
Delete selected variable
Show all device parameters at end of simulation in the audit trail
Select variables to save...
7
Run
Save
Cancel
Help
VDD
5.0V
R9
6.8kΩ
R10
16kΩ
C2
47uF
C1
0.01uF
U1
LM555CN
U8
4012BP_5V
R11
1.2kΩ
LED2
Multisim - July-13-20, 7:35:31 PM
Spreadsheet View
Results
Nets
Components
Copper layers
Simulation

Figure 4

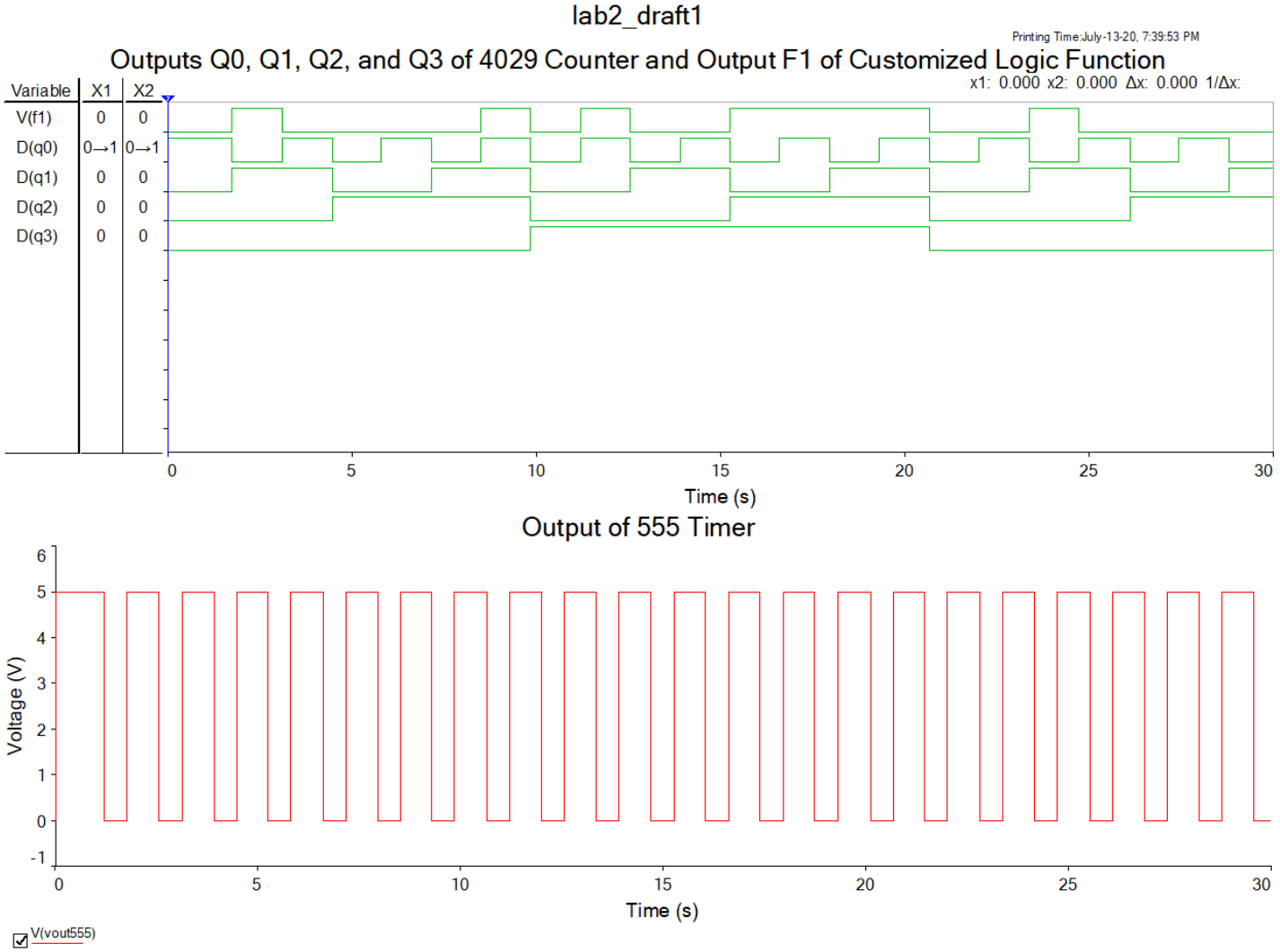

lab2_draft1
Printing Time:July-13-20, 7:39:53 PM
Outputs Q0, Q1, Q2, and Q3 of 4029 Counter and Output F1 of Customized Logic Function
x1: 0.000 x2: 0.000 Δx: 0.000 1/Δx:
Variable
X1
X2
V(f1) 0 0
D(q0) 0→1 0→1
D(q1) 0 0
D(q2) 0 0
D(q3) 0 0
0
5
10
15
20
25
30
Time (s)
Output of 555 Timer
Voltage (V)
6
5
4
3
2
1
0
-1
0
5
10
15
20
25
30
Time (s)
V(vout555)

Figure 5