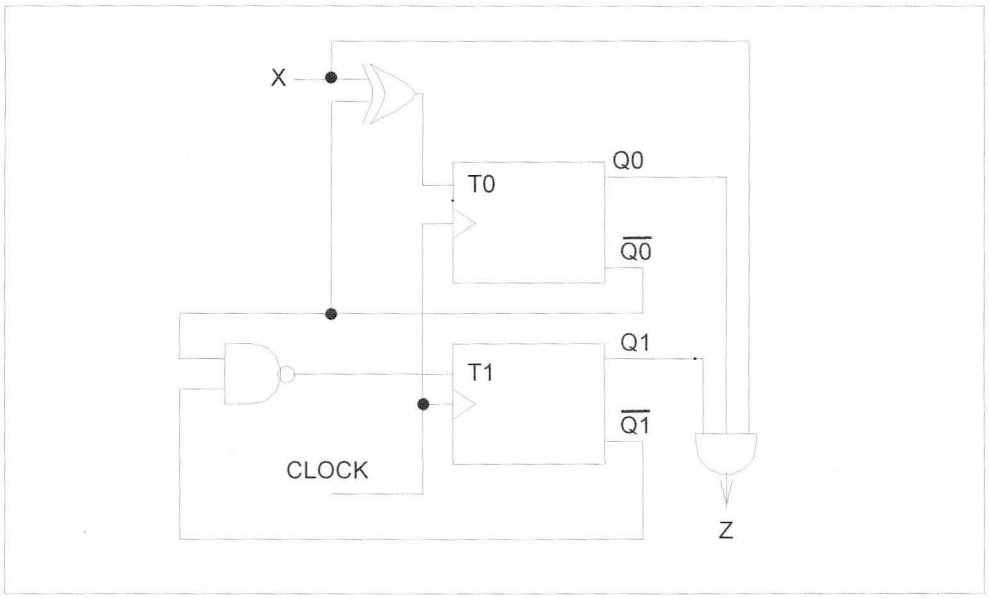
1. In the circuit below:

a) Is the design a MOORE or Mealy Model

b) Drive the state table assuming the states are: S0=00, S1=01, S2=10, S3=11

c) Draw the state diagram showing the state, input and output.



(a) Mealy design

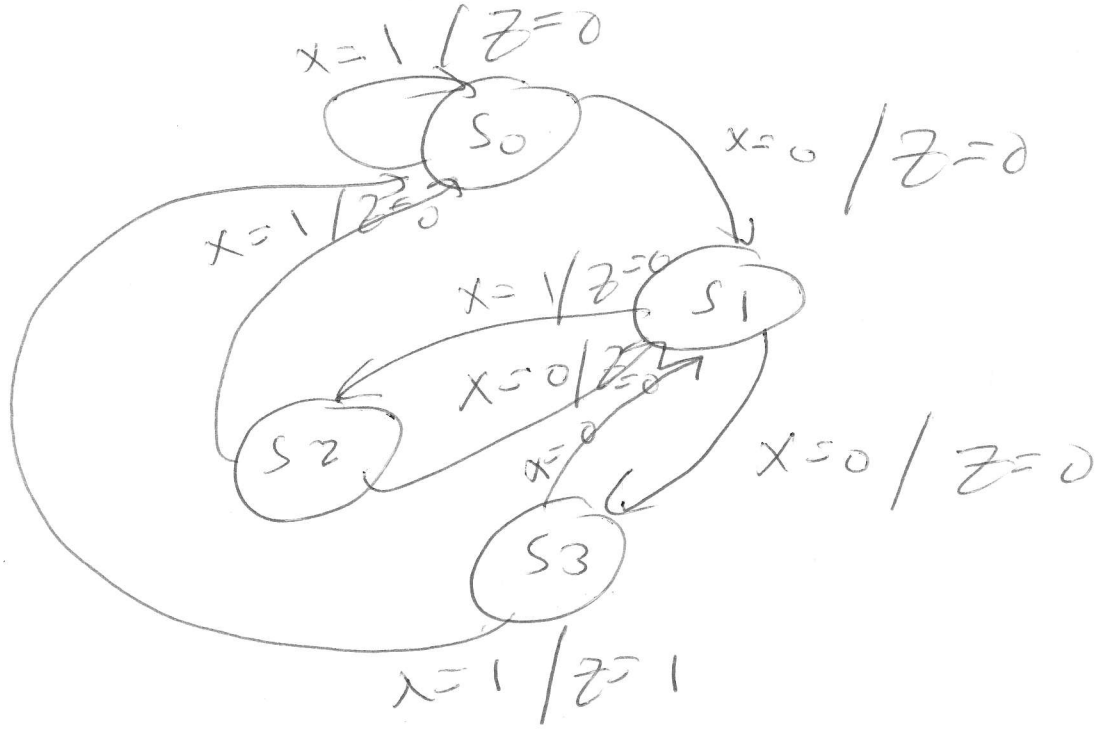
Name:_____ Section:_____

$T_0 = X \oplus \overline{Q_0}$

$T_1 = \overline{Q_0} \cdot \overline{Q_1} = Q_0 + Q_1$

$Z = X \cdot Q_0 \cdot Q_1$

P. state Q_1Q_0	X=0 N. state Q_1Q_0	T_1T_0	X=1 N. state Q_1Q_0	T_1T_0	Z X=0	Z X=1
S_0 00	01	01	S_1	00	S_0	0	0
S_1 01	10	11	S_3	11	S_2	0	0
S_2 10	11	01	S_1	10	S_0	0	0
S_3 11	10	01	S_1	11	S_0	0	1



Name:_____ Section:_____

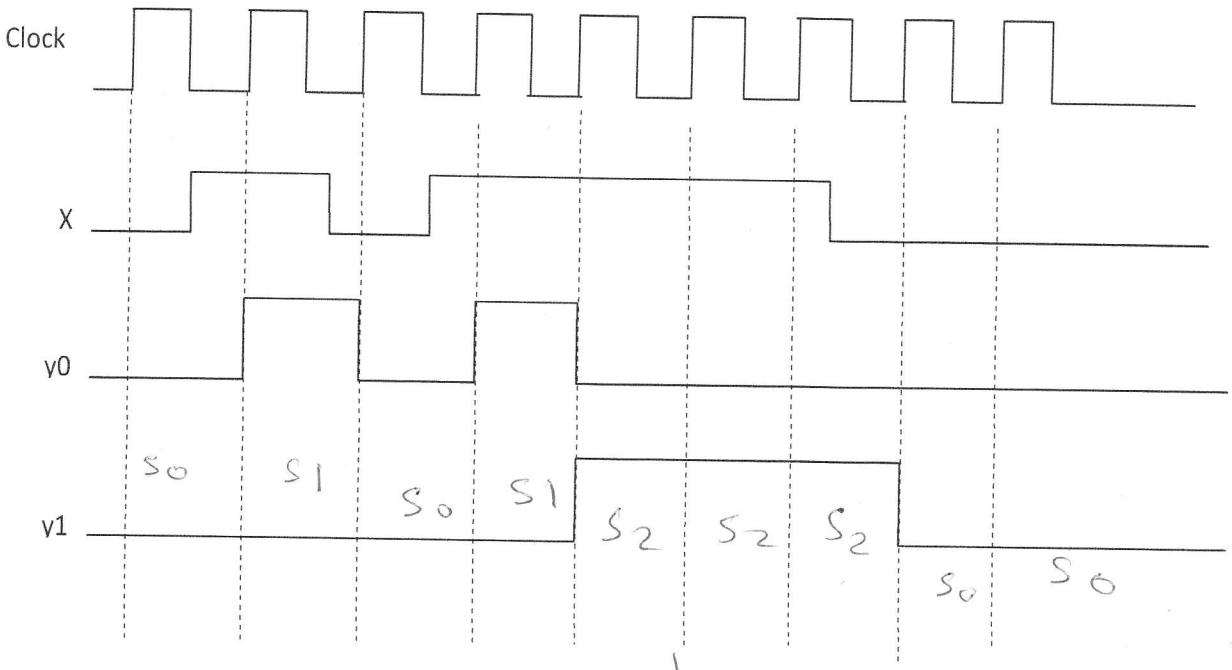
Name:_____ Section:_____

2. Given is the following timing diagram, clock signal, and input waveforms:

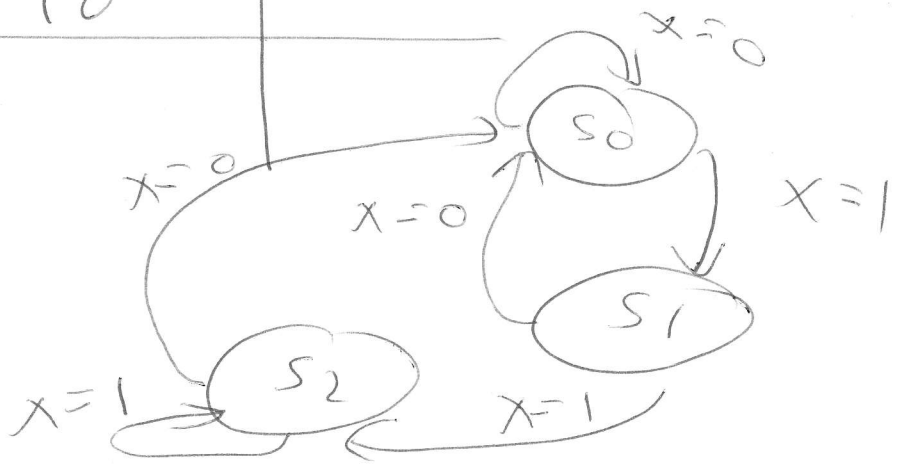
a) Derive the state-assigned table. (??marks)

b) Draw the state diagram (?? marks)

c) Drive the circuit that implement the FSM



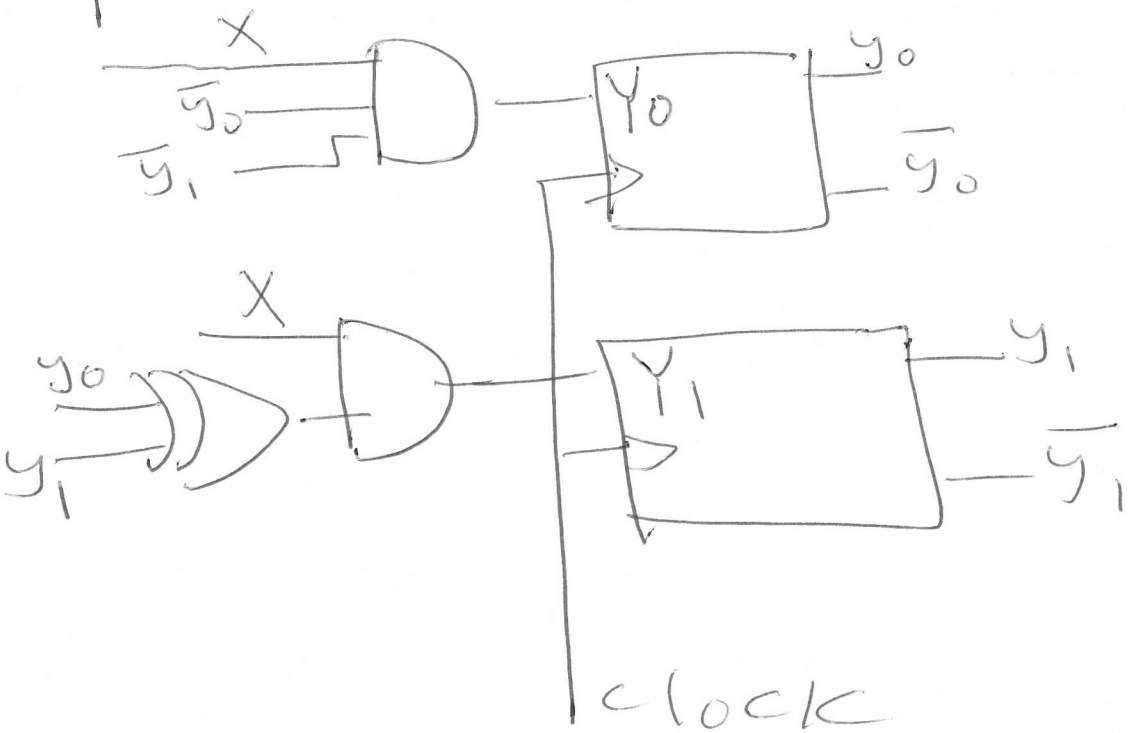
$y_1 y_0$	$X=0$	$X=1$
	$D_1 D_0$	$D_1 D_0$
S0 00	00	01
S1 01	00	10
S2 10	00	10



Name:_____ Section:_____

$Y_0 = \bar{y}_1 \cdot \bar{y}_0 \cdot X$

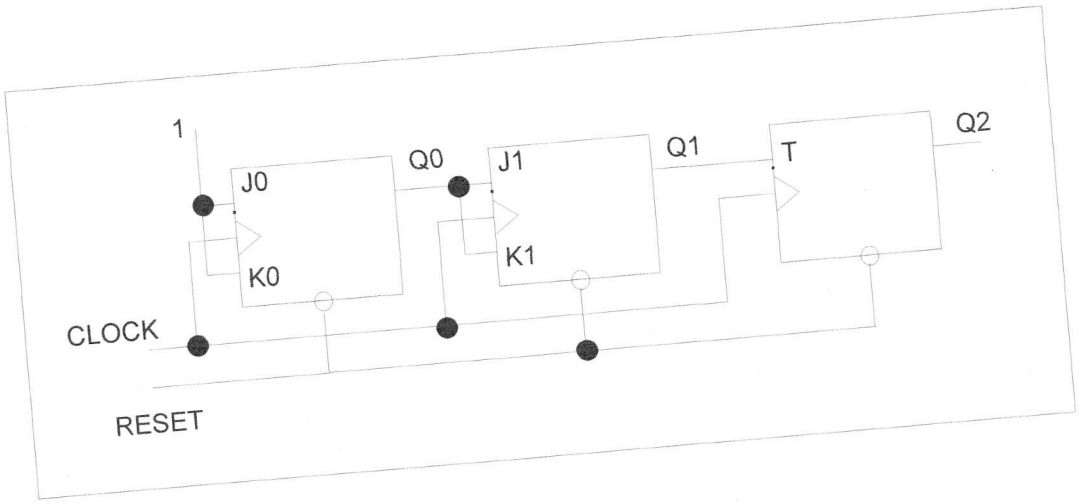
$Y_1 = X(\bar{y}_1 \cdot y_0 + y_1 \cdot \bar{y}_0)$

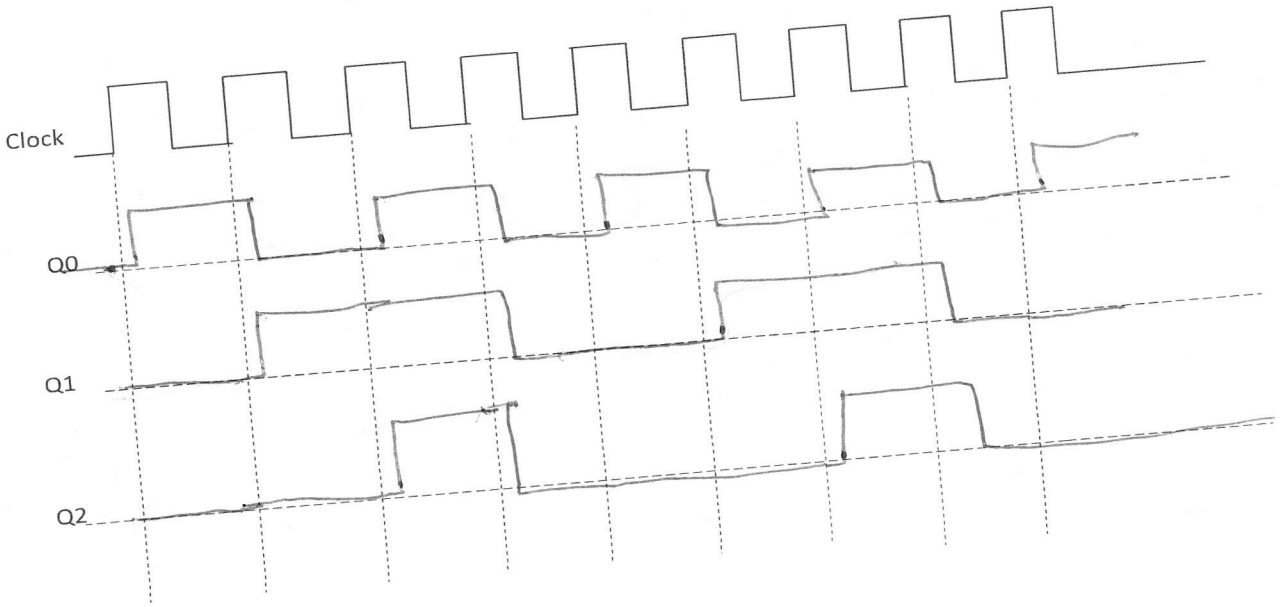


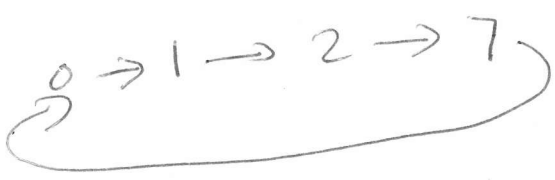
Name:_____ Section:_____

3. Following circuit is a counter

a) Complete the timing diagram of the counter starting from $Q_2Q_1Q_0 = 000$

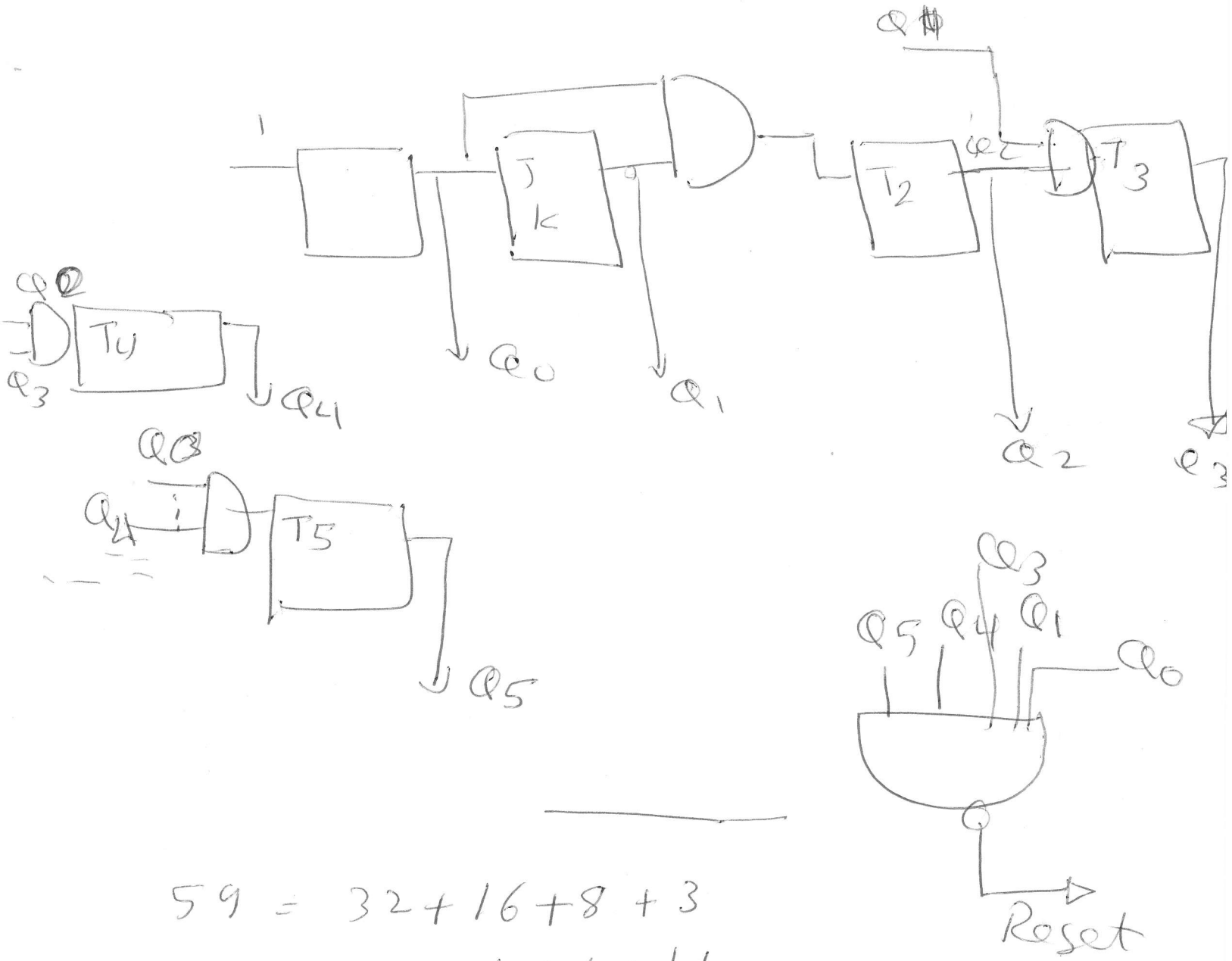






Name:_____ Section:_____

b) Change the design of the counter to a modulo-59 counter.



$59 = 32 + 16 + 8 + 3$

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