Toronto Metropolitan University

Department of Electrical, Computer and Biomedical Engineering

COE 328 – Digital Systems

Lab 3 - Adder and Subtractor Unit (2 weeks)

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1 Objectives:

- In this lab you will build a 4-bit adder-subtractor unit (ASU) and a combinational circuit using Altera FPGA chip.
- You will prepare and compile a VHDL file to implement the circuits.
- The ASU will feed the combinational circuit, and the output of the combinational circuit will be displayed on two 7-segnment displays (see Figure 1). The function of the combinational circuit will depend on the student ID number.

2 Pre-Lab Preparation

1. Modify the VHDL file of Figure 5.28 of the course textbook (3rd edition) to implement a 4-bit ASU represented in Figure 5.13 (see course textbook). Create a file ASU.vhd to accomplish this task. **Note:** change *ieee.std_logic_signed.all* to *ieee.std_logic_unsigned.all*.
2. Copy the code that implements a (unsigned) BCD-to-7-segment converter from Figure 6.47 (course textbook) into a file *sseg.vhd.*
3. Modify the *sseg.vhd* file so that the new (signed) BCD-to-7-segment converter could display the signed BCD digit (0-F) on two 7-segment displays. The right display must indicate the magnitude of the BCD digit, and left display must indicate the sign: "–" for negative numbers (the middle horizontal segment turned-on), and "no-sign" for positive numbers (all segments turned-off).
4. Minimize the logic expressions for your customized signals L_0, L_1, L_2, L_3 (see the combinational circuit C in Figure 1).

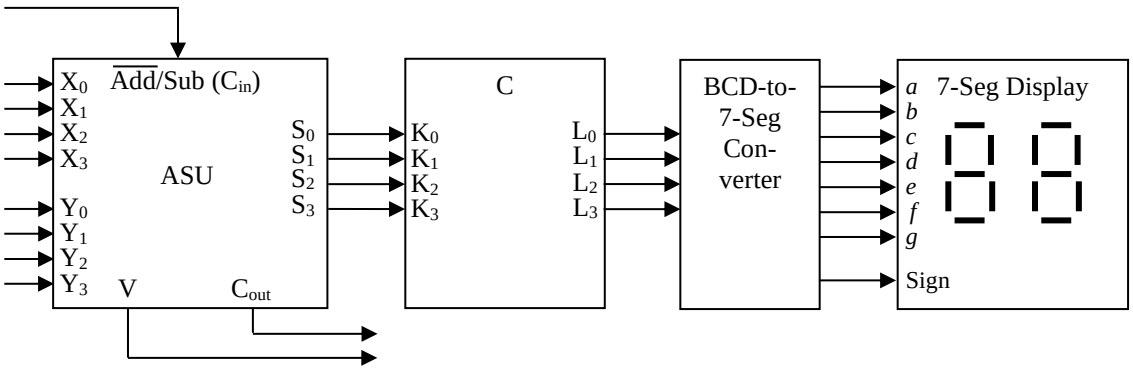

Figure 1

5. Create a new VHDL file *C.vhd* to implement the minimized logic expressions for the L_0, L_1, L_2, L_3 signals that correspond to a 4-bit BCD representation of your student ID digits (see **Part B**, item 2 below). The minimized logic expressions for these signals are obtained using K-Maps.

6. Using Functional Simulator, verify the circuit described by the VHDL file obtained in step 3. Set the signals: X_3, X_2, X_1, X_0, Y_3, Y_2, Y_1, Y_0, C_{in}, and observe the signals S_3, S_2, S_1, S_0, C_{out}, V (Overflow). The magnitude of the sum must be displayed on the right 7-segment display, and the sign of the sum must be displayed on the left 7-segment display.

3 Laboratory Work

The work is divided into two parts.

Part A

1. This part must be completed during the week 1 of this lab experiment
2. Compile your 4-bit Adder/Subtractor unit (ASU) file *ASU.vhd* and create a symbol file *ASU.bsf*
3. Compile your 7-segment code *sseg.vhd* as a separate project and create a symbol file *sseg.bsf*
4. Start a new Project **CombinedASU1** and create a block schematic file *CombineASU1.bdf*
5. Import the symbols **ASU** and **sseg** into the block schematic file *CombinedASU1.bdf*
6. Complete the wiring according to Figure 1 (excluding the combinational circuit C). Your design should look like the one represented in Figure 2.
7. Assign the following signals to the dedicated I/O-pins of the Altera Cyclone-II EP2C35F672C6 FPGA on the DE2 Development Board using *Pin Planner* (see Appendix C2 of the reference text):
   a) X_3, X_2, X_1, X_0, Y_3, Y_2, Y_1, Y_0 to SW7, SW6, …, SW1, SW0 (see *Complete Pin Planner-Altera.pdf* document on D2L or course web page)
   b) C_{in} to Pushbutton[0]
   c) S_3, S_2, S_1, S_0, to the Right/Left 7-segment displays, V (overflow) and C_{out} to LED Red[1] and LED Red[0] respectively

   Note: 1. All of the LEDs are of common anode type (active LOW)
   2. All of the 7-segment displays are of common cathode type (active HIGH)
8. Recompile the design and implement/program it into the Cyclone-II EP2C35F672C6 FPGA
9. Test your design and demonstrate the results to the lab instructor

   Note: The combinational circuit C is not used in this part of the assignment

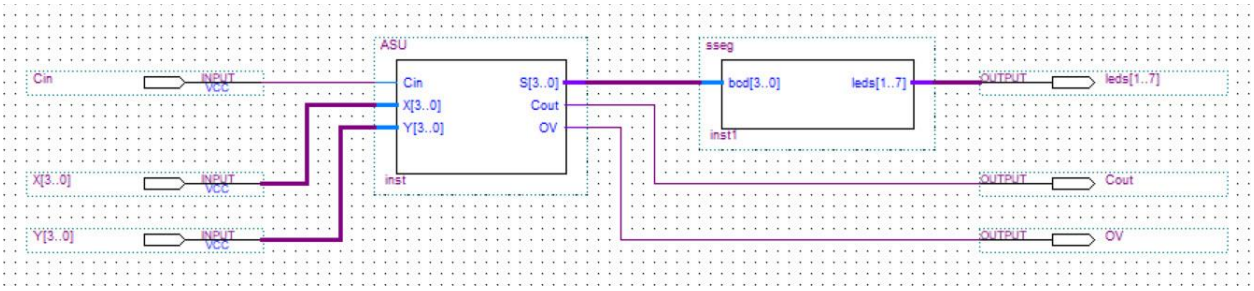

Figure 2

Part B

1. This part must be completed during the week 2 of this lab experiment
2. Consider the 9 digits of the student identifier D = {d_1, d_2, d_3, d_4, d_5, d_6, d_7, d_8, d_9} in its general representation. Write a table that represents each digit of your student ID in a BDC form (4 bits). For example, if a student's ID is: 111726015, it will consist of the following patterns: {0001, 0001, 0001, 0111, …, 0101} as depicted in Table 1
3. Compile your customized combinational circuit *C.vhd* and create a symbol file *c.bsf*
4. Start a new project **CombinedASU2** and create a block schematic file *CombinedASU2.bdf*
5. Import the symbols **ASU, C** and ***sseg*** (refer to **Part A**) into the block schematic file *CombinedASU2.bdf*
6. Complete the wiring according to Figure 1 (including the combinational circuit C)
7. Repeat the steps **7-9** from **Part A**

Table 1 (*d* represents "don't care" states)

S (ASU Output)				Stud. ID in BCD (C Output)				Stud. ID in DEC
S_3	S_2	S_1	S_0	L_3	L_2	L_1	L_0	d_i
0	0	0	0	0	0	0	1	1 (d_1)
0	0	0	1	0	0	0	1	1 (d_2)
0	0	1	0	0	0	0	1	1 (d_3)
0	0	1	1	0	1	1	1	7 (d_4)
0	1	0	0	0	0	1	0	2 (d_5)
0	1	0	1	0	1	1	0	6 (d_6)
0	1	1	0	0	0	0	0	0 (d_7)
0	1	1	1	0	0	0	1	1 (d_8)
1	0	0	0	0	1	0	1	5 (d_9)
1	0	0	1	*d*	*d*	*d*	*d*	
…	…	…	…	*d*	*d*	*d*	*d*	
1	1	1	1	*d*	*d*	*d*	*d*	