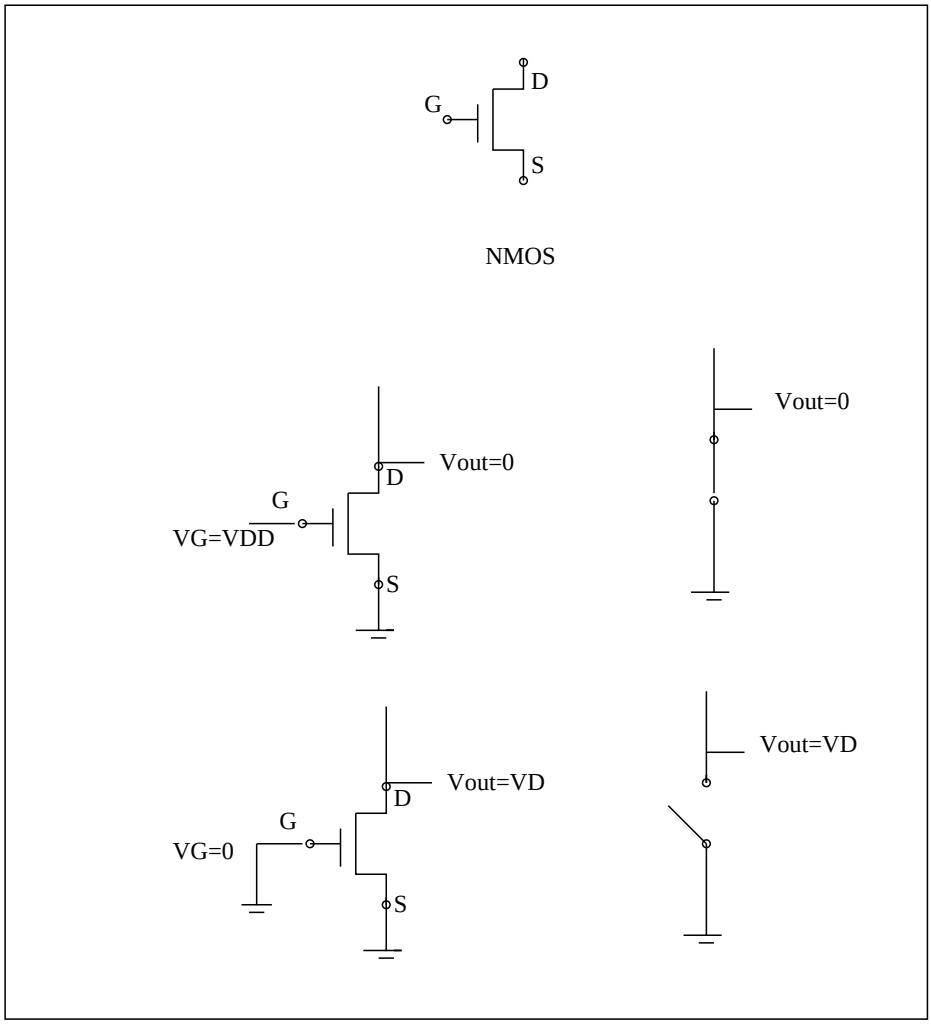
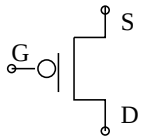
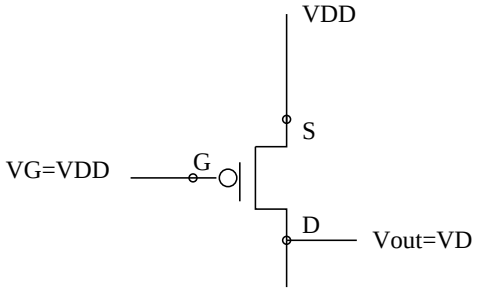
Implementation Technology
Transistor Switches
1-NMOS Transistor

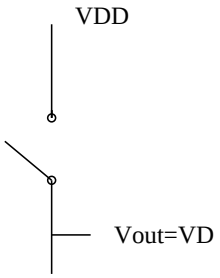


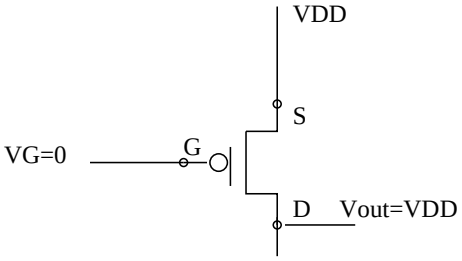
2-PMOS Transistor

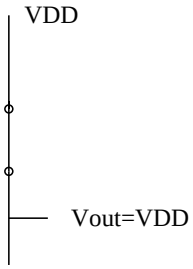


PMOS

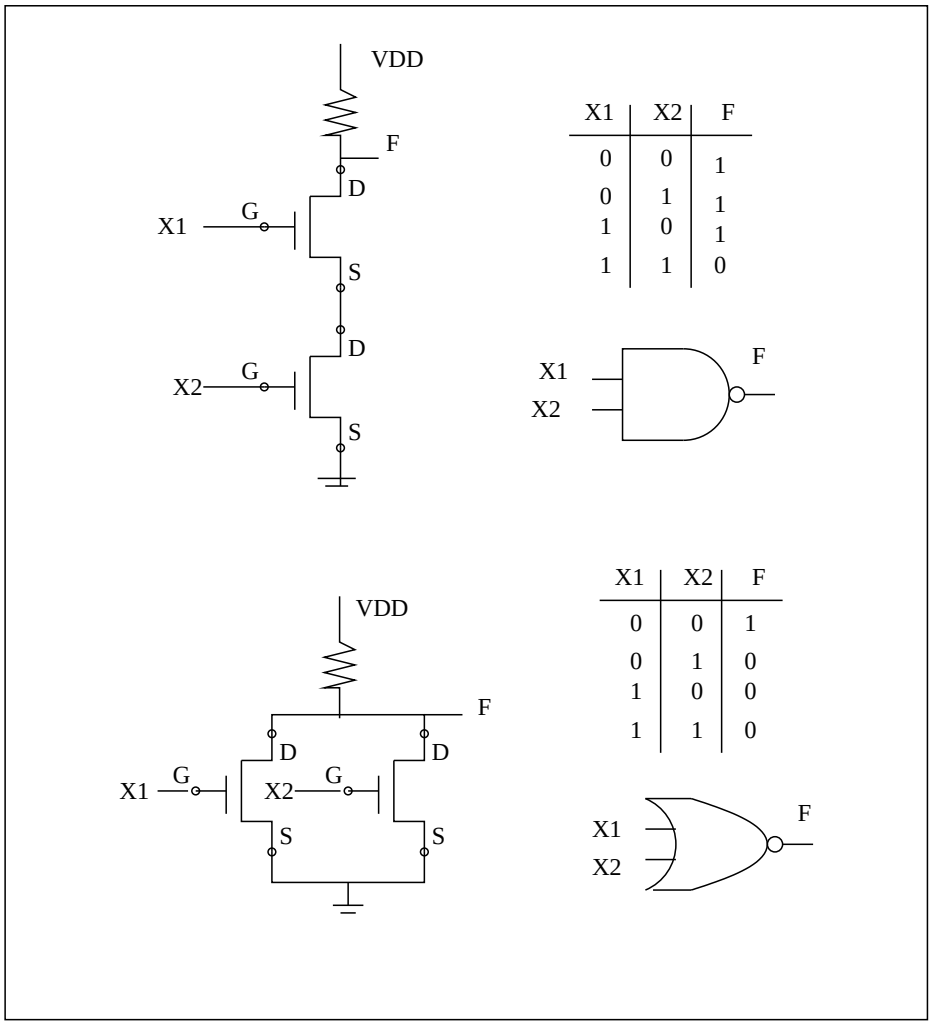








NMOS Logic Gates



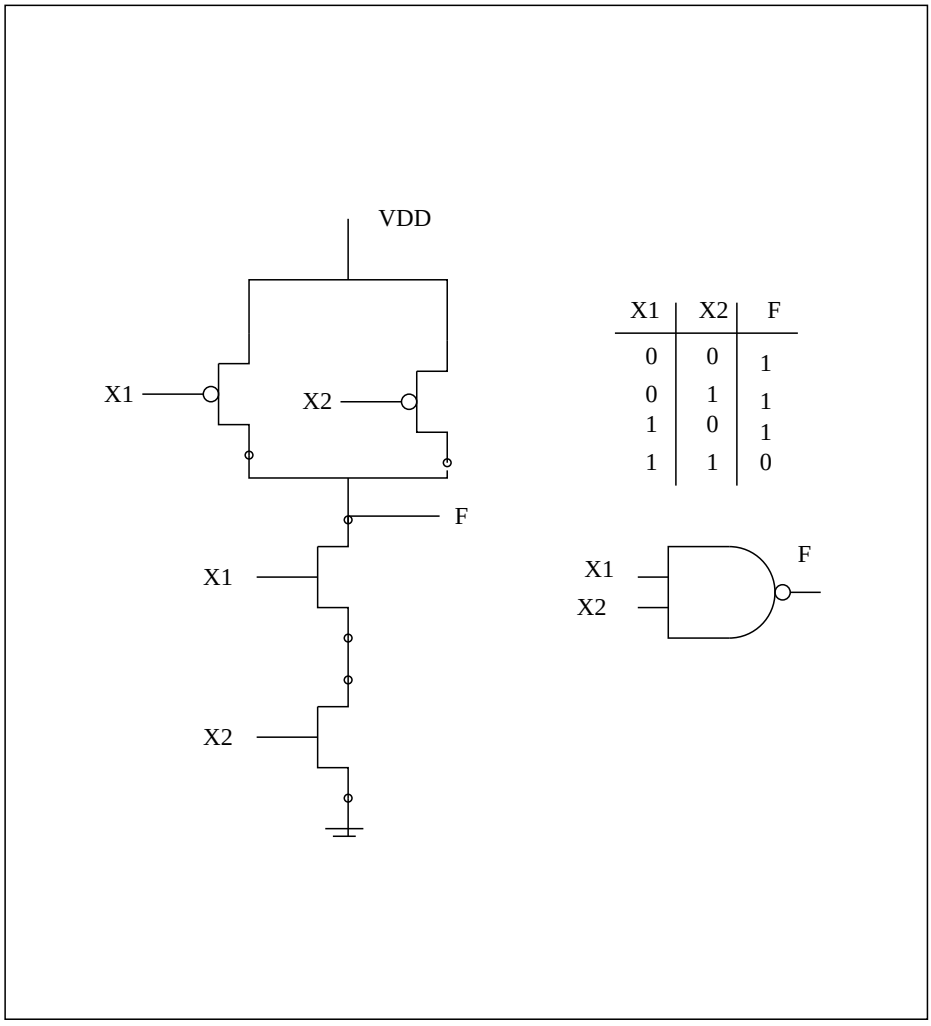
CMOS Logic Gates

- Replace Pull Up resistor by PMOS Transistor
- PMOS Circuit and NMOS Circuit are Complement of each other
- Use DeMorgan to drive NMOS Circuit from PMOS circuit
- One circuit ON, Other OFF

Example: CMOS NAND Gate

F= !(X1.X2)= !X1 + !X2

NMOS = !(!(X1.X2)) = X1.X2



X1	X2	F
0	0	1
0	1	1
1	0	1
1	1	0

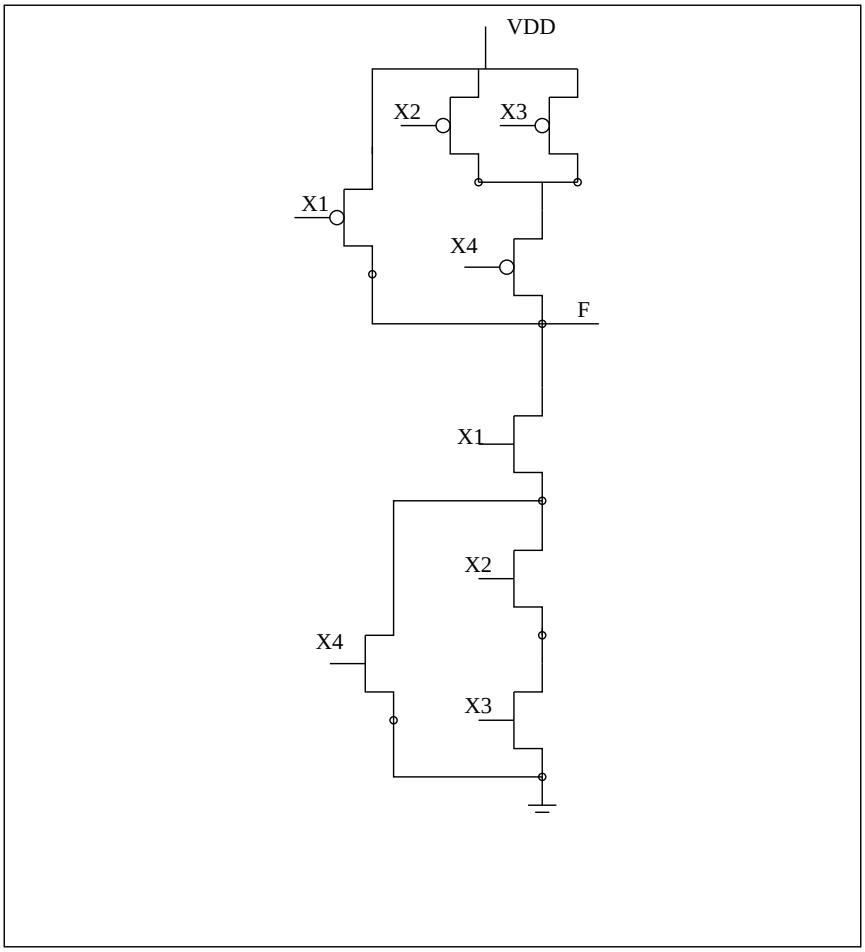
Example: Implement using CMOS Circuit

F= !X1 + (!X2 + !X3).!X4

NMOS = !(!X1 + (!X2 + !X3).!X4)

=X1.!((!X2 + !X3).!X4))

=X1.(X2.X3+X4)



Standard Chips

Old technology: 7400 (TTL) chips that include standard gates

Example : 7408 has 4 AND gates

Takes space, not flexible and consumes more power

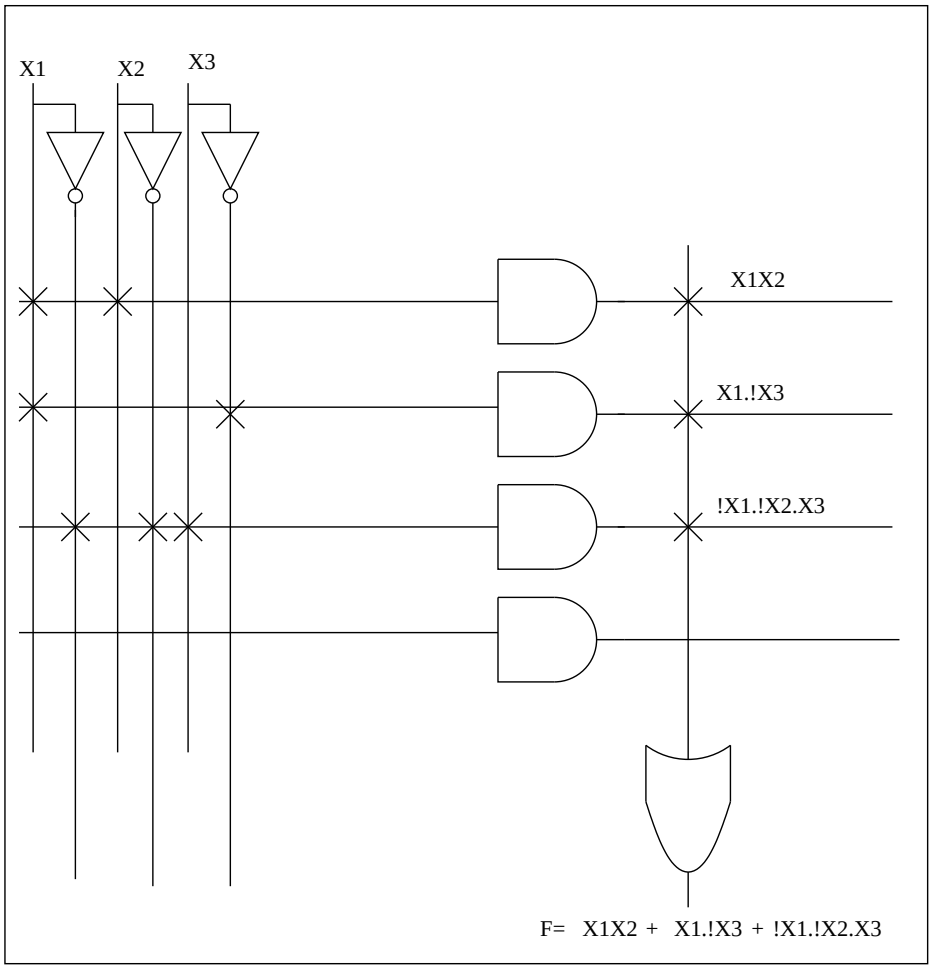
PLA: Programmable Logic Arrays

Two arrays: AND Plane, OR Plane

Could implement any function using Sum of Products

Example: Implement in PLA F= X1.X2 + X1.!X3 + !X1.!X2.X3

PLA: Programmable Logic Arrays



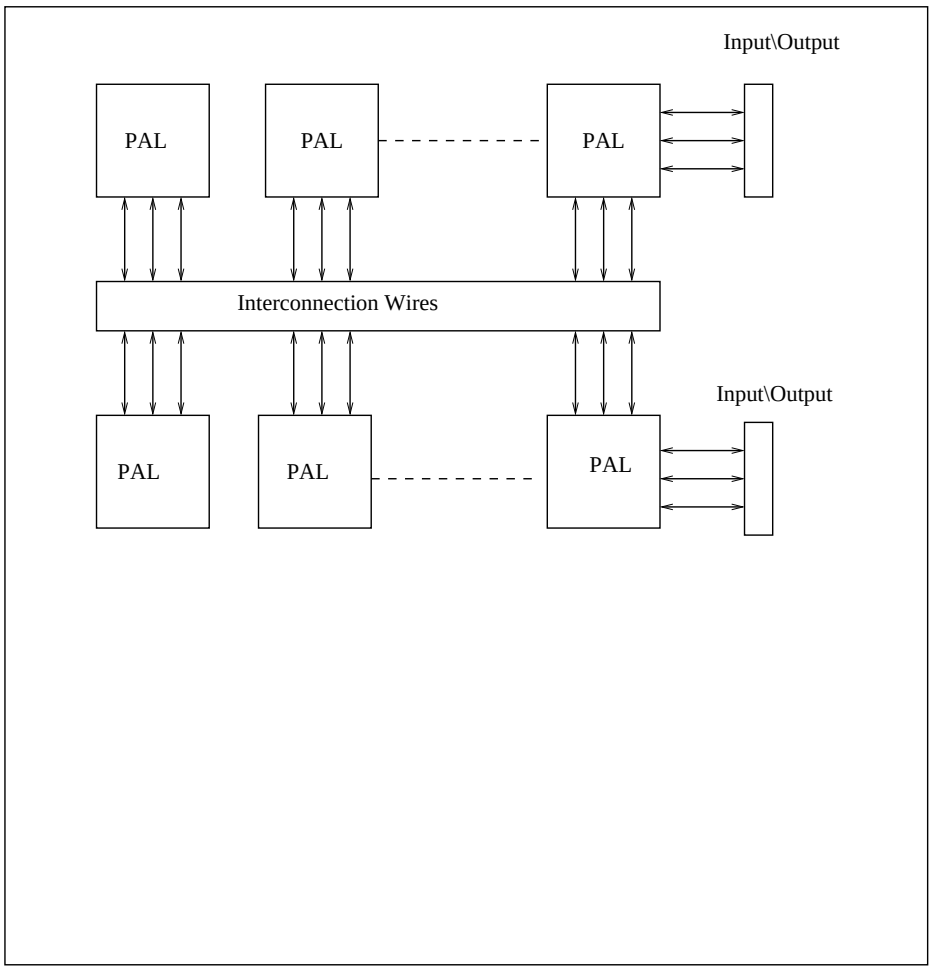
Programmable Array Logic " PAL"

ONLY the AND Plane is Programmable OR Plane is fixed

Simple, fast, reduces cost of implementation

CPLD: Complex Programmable Logic Devices

Multiple PALS



Programming

- Compile code for design using CAD Tools
  This produces FUSE Map file
- Transfer this file to PROGRAMMER
- Configure Programmer for device and Insert Device
- Program Device and Verify it

JITAG Programming

When Chip is built in system,
use a JITAG PORT to transfer fuse map to device
then program device in chip

FPGA: Field Programmable Gate Arrays

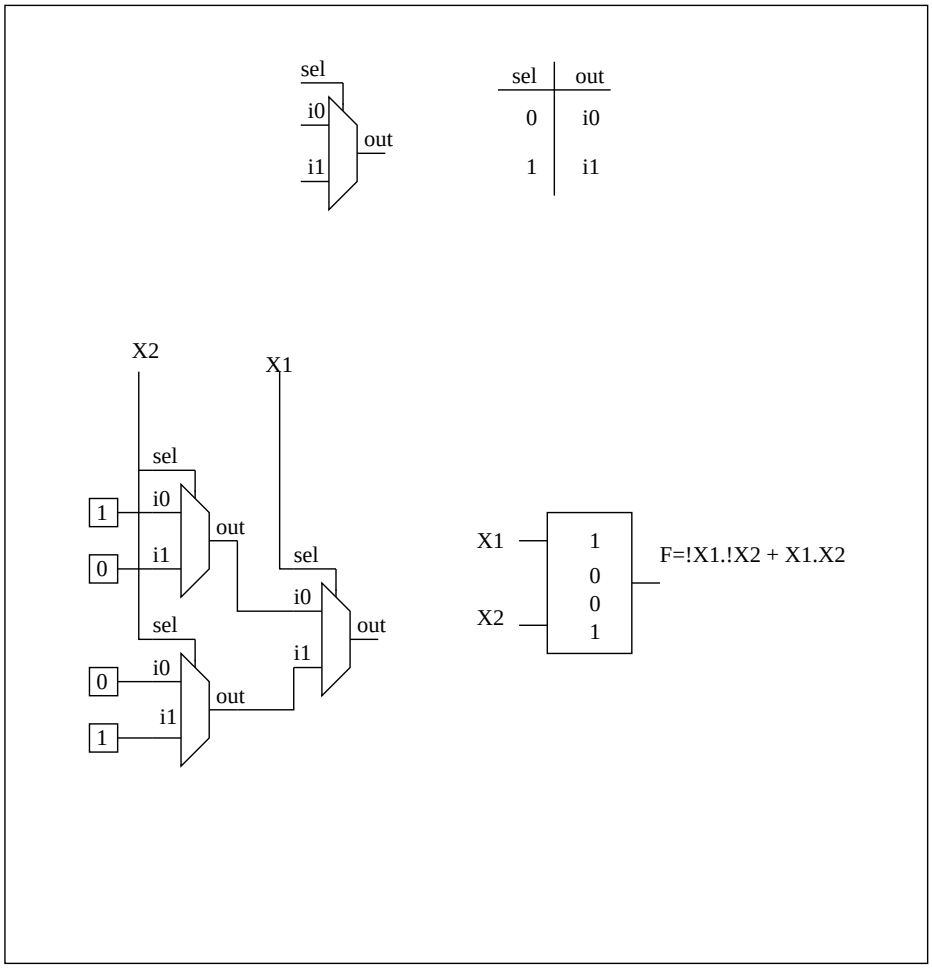
Uses array of Logic Blocks (no AND OR Planes)

Each Logic block is a Look Up Table (LUT)

LUT : has storage cells and multiplexer

FPGA uses much more gates to reduce number of chips

FPGA is Volatile (loses design if power OFF)



Practical Aspects

Characteristics of CMOS Inverter:

Noise Margin:

$NM_L = VI_L - VO_L$

$NM_H = VO_H - VI_H$

Example: Find NM_L, NM_H if $VO_H = 5V$, $VO_L = 0$ and $VI_L = 1V$, $VI_H = 3V$

$NM_L = 1 - 0 = 1$, $NM_H = 5 - 3 = 2$

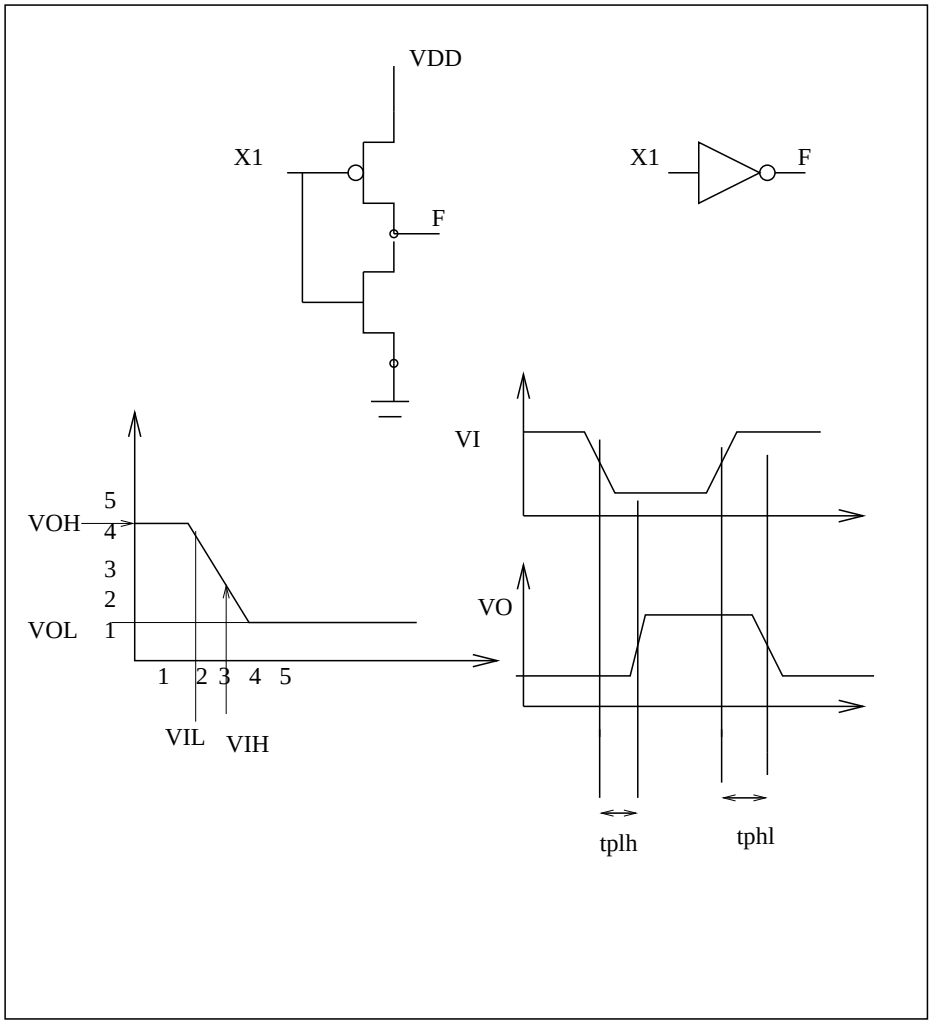
Time Delay: Delay TP_{LH} from (o) Level to (1)

Time Delay: Delay TP_{HL} from (1) Level to (0)

Power Dissipation: $P = CFVDD^2$

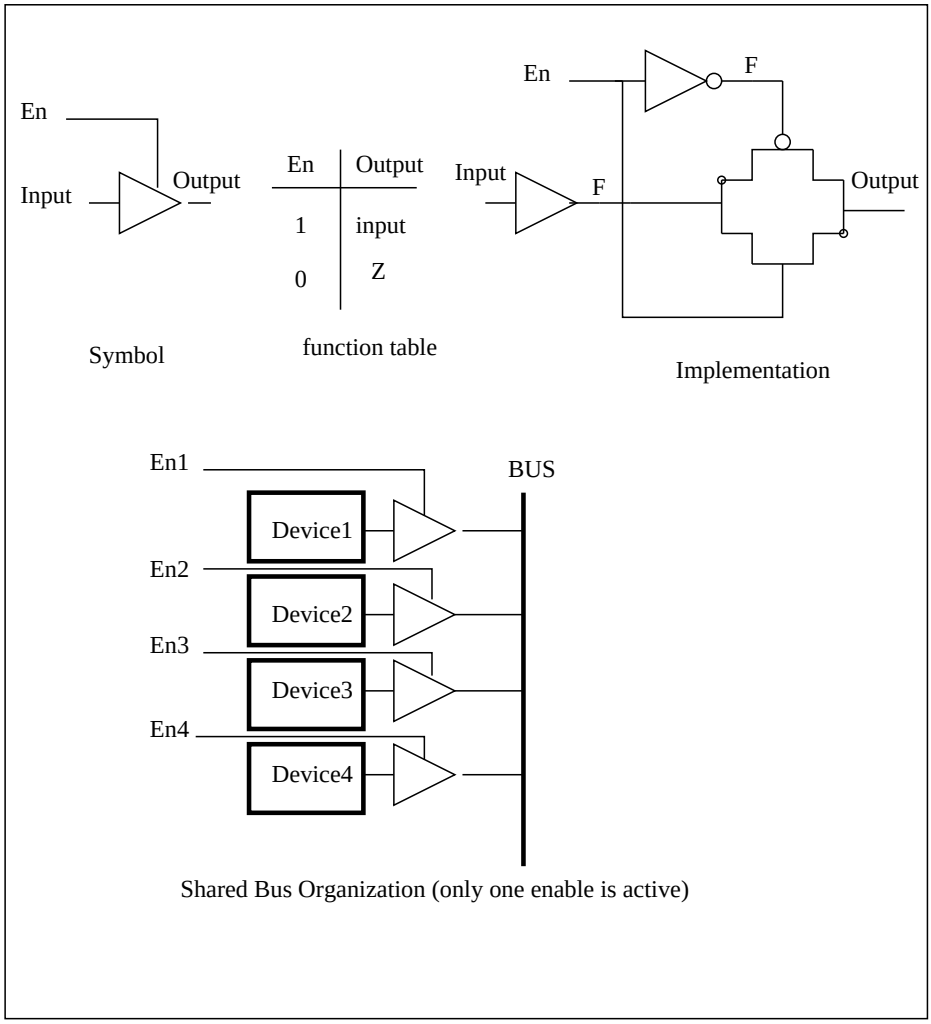
Fan In: Maximum number of inputs to the gate

Fan out: Maximum number of other gates that a specific gate drives



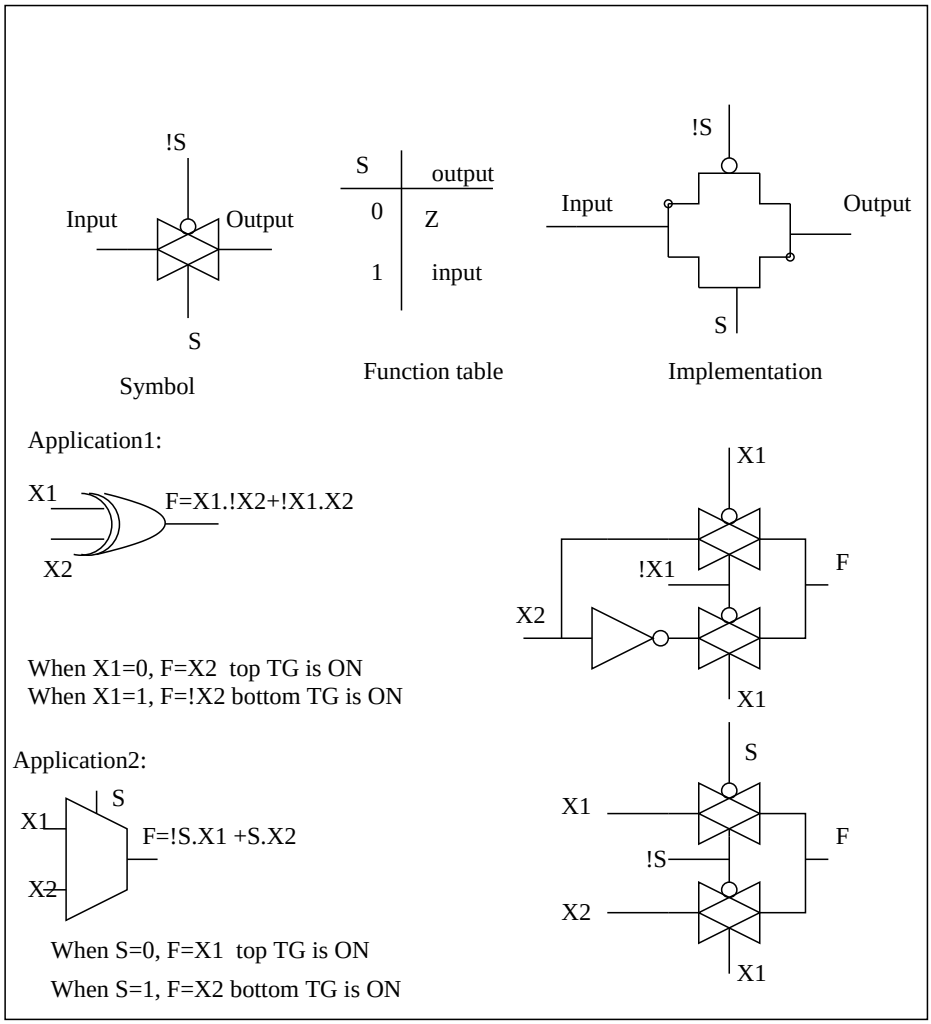
Tri-State Buffer

Used to connect diveces to shared BUS



Transimition Gates

Used to simplify some functions (XOR, MUX)

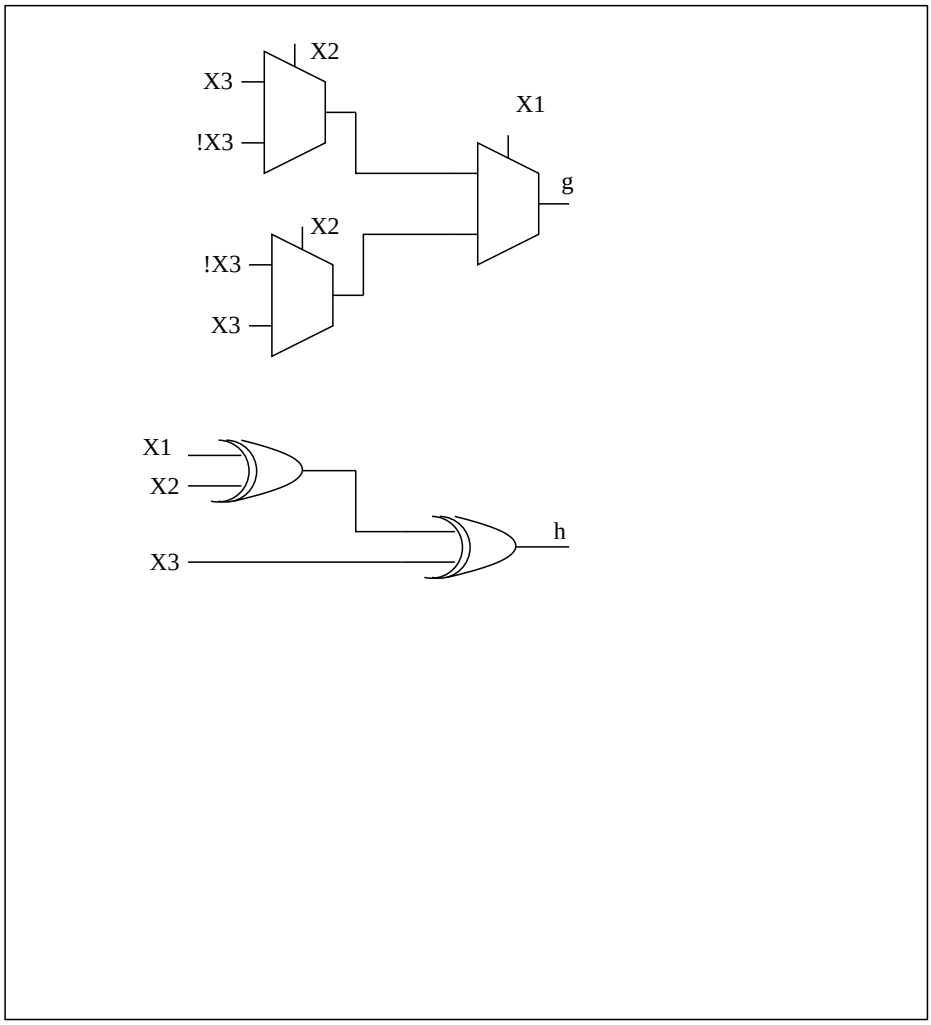


Problems from Ch3

- **3-3 a** Show that the two circuits have same function
  g=!X1.!X2.X3+!X1.X2.!X3+X1.!X2.!X3+X1.X2
  h=(X1.!X2+!X1.X2).!X3+!(X1.!X2+!X1.X2).X3
  =(X1.!X2+!X1.X2).!X3+(X1.X2+!X1.!X2).X3

- **3-3 b** Each XOR gate uses 2 inverters + 2 TG
  XOR gate needs 2x2 + 2x2 =8 transistors
  2 XOR gates need 16 transistors

- 3-3



- **3-4** Build a 6 input AND gate using NAND and NOR gates
  F=!!(X1.X2.X3.X4.X5.X6)
  =!(!(X1.X2.X3)+!(X4.X5.X6)

- **3-7**Find truth table for CMOS circuit
  drive logic function F= (!X1+!X2).!X3.!X4
  from PMOS
  simplest sum of product F= !X1.!X3.!X4 + !X2.!X3.!X4
  Cost 4 INV + 2 AND + 1 OR
  4X2 + 2X8 + 1X4= 28 transistor

- 3-4, 3-7