

## Course Outline (W2025)

### COE608: Computer Organization and Architecture

<b>Instructor(s)</b>	<p>Dr. Vadim Geurkov [Coordinator] Office: ENG430 Phone: (416) 979-5000 x 556088 Email: vgeurkov@torontomu.ca Office Hours: Thursday, 5 pm - 6 pm</p> <p>Demetres Kostas Office: TBA Phone: TBA Email: dee@torontomu.ca Office Hours: Wednesdays 13:30-14:30</p>
<b>Calendar Description</b>	<p>The main topics of the course include basic architecture of modern computers, interaction between computer hardware and software at various levels, and performance evaluation and metrics. Instruction set design, computer arithmetic is also discussed. Data path and control unit design for RISC Processors are covered in detail. The laboratory work includes the design and implementation of a 16-bit RISC CPU using an FPGA development system and VHDL.</p>
<b>Prerequisites</b>	CEN 199 and COE 328 and COE 538
<b>Antirequisites</b>	None
<b>Corerequisites</b>	None
<b>Compulsory Text(s):</b>	<ol style="list-style-type: none"> <li>1. Computer Organization and Design MIPS Edition. The Hardware/ Software Interface, David Patterson and John Hennessy, 6th edition 2020, Morgan Kaufmann Publishers, Elsevier Inc., ISBN 9780128201091 (4th or 5th editions can be also used)</li> <li>2. Laboratory Manuals and other Documents: Available through: D2L (primary source) and <a href="http://www.ee.ryerson.ca/~courses/coe608/">http://www.ee.ryerson.ca/~courses/coe608/</a> (older content)</li> <li>3. Lecture Slides available on D2L</li> </ol>
<b>Reference Text(s):</b>	<ol style="list-style-type: none"> <li>1. Computer Organization and Embedded Systems, 6th Edition, Carl Hamacher, Zvonko Vranesic, Safwat Zaky, Naraig Manjikian, McGrawHill , 2011, ISBN: 0073380652</li> <li>2. Embedded Core Design with FPGAs, Z. Navabi, McGraw Hill 2007, ISBN 978-0- 07-147481- 8.</li> <li>3. Logic and Computer Design Fundamentals, Morris Mano &amp; Charles R. Kime, 4th edition 2008 or latest edition, Prentice Hall.</li> </ol>
<b>Learning Objectives (Indicators)</b>	<p>At the end of this course, the successful student will be able to:</p> <ol style="list-style-type: none"> <li>1. Interconnect engineering concepts related to instruction set architecture, register transfer, interconnects like buses, 3-state buffers and Muxes as well as control hardware to design</li> </ol>

	<p>various processors. Learn to employ specialized knowledge of subsystems like data-path, memory and control unit components to design a RISC processing element. <b>(1c)</b></p> <p>2. Define processor specification and instruction set architecture. Solve various challenges of high performance RISC processor design in multiple stages by employing VHDL (CAD) based modeling and simulation methodologies to test and verify each stage of processor design and then integrate different stages into efficient processor architecture. <b>(4b), (4c), (4a)</b></p> <p>3. Demonstrate the main features of all the labs and answer CPU design related questions during the demo/oral sessions. Write lab and CPU design reports by following a standard IEEE like format, where all the reports are evaluated based on their completeness, English, and relevant contents. <b>(7a), (7b)</b></p> <p><b>NOTE:</b>Numbers in parentheses refer to the graduate attributes required by the Canadian Engineering Accreditation Board (CEAB).</p>												
<b>Course Organization</b>	<p>3.0 hours of lecture per week for 13 weeks</p> <p>2.0 hours of lab per week for 12 weeks</p> <p>0.0 hours of tutorial per week for 12 weeks</p>												
<b>Teaching Assistants</b>	<p>Daniel Segura (dsegura@torontomu.ca)</p> <p>Yasaman Ahmadiadli (yahmadiadli@torontomu.ca)</p> <p>Protik Mukherjee (protik.mukherjee@torontomu.ca)</p> <p>Tajinderpal Toor (ttoor@torontomu.ca)</p> <p>Paul Economou (paul.economou@torontomu.ca)</p>												
<b>Course Evaluation</b>	<table border="1"> <thead> <tr> <th colspan="2">Theory</th></tr> </thead> <tbody> <tr> <td>Midterm Exam</td><td>30 %</td></tr> <tr> <td>Final Exam</td><td>40 %</td></tr> </tbody> </table> <table border="1"> <thead> <tr> <th colspan="2">Laboratory</th></tr> </thead> <tbody> <tr> <td>Labs with formal reports</td><td>30 %</td></tr> <tr> <td><b>TOTAL:</b></td><td><b>100 %</b></td></tr> </tbody> </table> <p><b>Note:</b> In order for a student to pass a course, a minimum overall course mark of 50% must be obtained. In addition, for courses that have both "<b>Theory and Laboratory</b>" components, the student must pass the Laboratory and Theory portions separately by achieving a minimum of 50% in the combined Laboratory components and 50% in the combined Theory components. Please refer to the "<b>Course Evaluation</b>" section above for details on the Theory and Laboratory components (if applicable).</p>	Theory		Midterm Exam	30 %	Final Exam	40 %	Laboratory		Labs with formal reports	30 %	<b>TOTAL:</b>	<b>100 %</b>
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<b>Examinations</b>	<p>Midterm exam will be in Week 7 or 8, 1.5 hours, closed book (Weeks 1-7 lectures and labs will be covered).</p> <p>Final exam will include all course materials.</p>												
<b>Other Evaluation Information</b>	None												
<b>Teaching Methods</b>	lecture time: Tuesday, 8-11am, DCC-208, DCC-204												
<b>Other Information</b>	None												

## Course Content

Week	Hours	Chapters / Section	Topic, description
1	3		Introduction Computer Systems Technology: Computer Organization VHDL
2	3		Computer Performance: Performance metrics and evaluation
3	3		Instruction set Design: -Instruction representation, -Arithmetic and Logic Operations
4	3		Instruction set Design: -Addressing modes, -Branching
5	3		Input Output Systems
6	3		Software: Assembler, Compiler, Linker, and Loader
7	3		Datapath: -Register transfer, -ASM Chart and Control Unit Design -Single and Multi-cycle CPU Data-path Design
8	3		Pipelining: -Data Hazards, -Branch hazards, -Stalls and Forwarding

9	3		Memory Hierarchy
10	3		Memory and Cache System
11	3		Arithmetic for computers: Integer arithmetic operations
12	3		Arithmetic for computers: ALU Design and Implementation
13	3		Catching up and Review

### Laboratory(L)/Tutorials(T)/Activity(A) Schedule

Week	L/T/A	Description
2	ENG408	Lab1: Quartus-II FPGA Development Environment and Introduction to VHDL
3	ENG408	Lab 2: Program counter and Register set design: VHDL code Design and Simulation.
4	ENG408	Lab 3a: 32-bit ALU: VHDL design and simulation.
5	ENG408	Lab 3b: ALU Implementation on Altera Cyclone-IV and Testing
6	ENG408	Lab 4a: Data Memory Module Design and Implementation
7	ENG408	Lab 4b: CPU Datapath Design
8	ENG408	Lab 4b: CPU Datapath Design and Simulation

9	ENG408	Lab 4b: CPU Datapath Simulation and Submission Lab 5: CPU Control Unit Design
10	ENG408	Lab 5: CPU Control Unit Design
11	ENG408	Lab 5: CPU Control Unit - Submission Lab 6: Overall CPU Project - Integration and simulation of CPU.
12	ENG408	Lab 6: Integration and simulation of CPU. Fine-tuning and submission. Overall CPU Project Demonstration and Oral
13	ENG408	Overall CPU Project Bonus Demonstration and Oral

## University Policies & Important Information

Students are reminded that they are required to adhere to all relevant university policies found in their online course shell in D2L and/or on [the Senate website](#)

Refer to the [Departmental FAQ page](#) for further information on common questions.

## Important Resources Available at Toronto Metropolitan University

- [The Library](#) provides research [workshops](#) and individual assistance. If the University is open, there is a Research Help desk on the second floor of the library, or students can use the [Library's virtual research help service](#) to speak with a librarian.
- [Student Life and Learning Support](#) offers group-based and individual help with writing, math, study skills, and transition support, as well as [resources and checklists to support students as online learners](#).
- You can submit an [Academic Consideration Request](#) when an extenuating circumstance has occurred that has significantly impacted your ability to fulfill an academic requirement. You may always visit the [Senate website](#) and select the blue radio button on the top right hand side entitled: **Academic Consideration Request (ACR)** to submit this request.

*For Extenuating Circumstances, Policy 167: Academic Consideration allows for a once per semester ACR request without supporting documentation if the absence is less than 3 days in duration and is not for a final exam/final assessment. Absences more than 3 days in duration and those that involve a final exam/final assessment, require documentation. Students must notify their instructor once a request for academic consideration is submitted. See Senate [Policy 167: Academic Consideration](#).*

- If taking a remote course, familiarize yourself with the tools you will need to use for remote learning. The [Remote Learning Guide](#) for students includes guides to completing quizzes or exams in D2L Brightspace, with or without [Respondus LockDown Browser and Monitor, using D2L Brightspace](#), joining online meetings or lectures, and collaborating with the Google Suite.
- Information on Copyright for [Faculty](#) and [students](#).

## Accessibility

- Similar to an [accessibility statement](#), use this section to describe your commitment to making this course accessible to students with disabilities. Improving the accessibility of your course helps minimize the need for accommodation.
- Outline any technologies used in this course and any known accessibility features or barriers (if applicable).
- Describe how a student should contact you if they discover an accessibility barrier with any course materials or technologies.

## Academic Accommodation Support

Academic Accommodation Support (AAS) is the university's disability services office. AAS works directly with incoming and returning students looking for help with their academic accommodations. AAS works with any student who requires academic accommodation regardless of program or course load.

- Learn more about [Academic Accommodation Support](#).
- Learn [how to register with AAS](#).

Academic Accommodations (for students with disabilities) and Academic Consideration (for students faced with extenuating circumstances that can include short-term health issues) are governed by two different university policies. Learn more about [Academic Accommodations versus Academic Consideration and how to access each](#).

## Wellbeing Support

At Toronto Metropolitan University, we recognize that things can come up throughout the term that may interfere with a student's ability to succeed in their coursework. These circumstances are outside of one's control and can have a serious impact on physical and mental well-being. Seeking help can be a challenge, especially in those times of crisis.

If you are experiencing a mental health crisis, please call 911 and go to the nearest hospital emergency room. You can also access these outside resources at anytime:

- **Distress Line:** 24/7 line for if you are in crisis, feeling suicidal or in need of emotional support (phone: 416-408-4357)
- **Good2Talk:** 24/7-hour line for postsecondary students (phone: 1-866-925-5454)
- **Keep.meSAFE:** 24/7 access to confidential support through counsellors via [My SSP app](#) or 1-844-451-9700

If non-crisis support is needed, you can access these campus resources:

- **Centre for Student Development and Counselling:** 416-979-5195 or email [csdc@torontomu.ca](mailto:csdc@torontomu.ca)
- **Consent Comes First - Office of Sexual Violence Support and Education:** 416-919-5000 ext 3596 or email [osvse@torontomu.ca](mailto:osvse@torontomu.ca)
- **Medical Centre:** call (416) 979-5070 to book an appointment

We encourage all Toronto Metropolitan University community members to access available resources to ensure support is reachable. You can find more resources available through the [Toronto Metropolitan University Mental Health and Wellbeing](#) website.