COE758 – Digital Systems Engineering

Project #2 – Simple Video Game Processor for VGA

Objectives

- To learn the functionality of video-output subsystem and Video Graphic Adaptor (VGA) standard as well as on-chip (FPGA) to I/O device interfacing.
- To get practical experience in design and implementation of the real-time high-performance signal generators implemented on-chip (FPGA) with custom logic circuits. Getting hands-on experience in interfacing the on-chip circuits with external real-time I/O devices (VGA Monitor).
- To learn VHDL-coding technique for real-time applications in the environment of Xilinx ISE CAD system and hardware evaluation platform based on Xilinx Spartan-3E FPGA.

Background

Provided in handouts

Specification

The Simple Video-Game Processor (SVGP) should provide:

1. Static video-frame – game field in green color with white borders as shown in Figure 1:

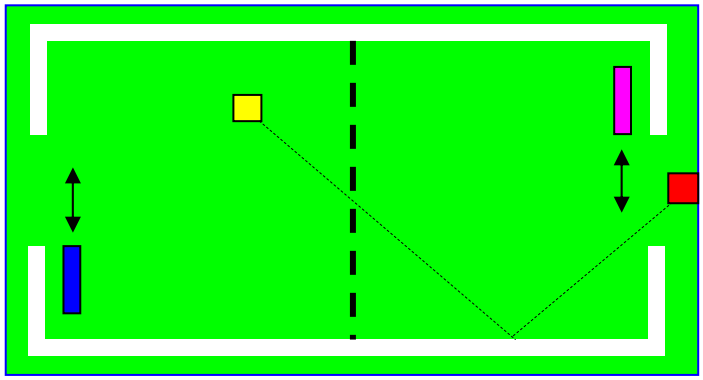

Figure 1: Static SVGP video-frame with dynamic elements– "ball" and "players"

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2. Dynamic elements: i) yellow "ball" which can "fly" on the field between the borders reflecting from borders and from players; ii) players in "blue" and "ping" colors which can move up and down being controlled by switches on the board accordingly.

3. Behavior: i) when ball hits the boarder or "player" it changes its trajectory as of ± 90 angular degrees according to the direction of hit (e.g. from down to up when hitting the bottom border, etc.); ii) when ball pass the "gate" on left or right hand side it changes it color to red and disappears while passing the video-frame. Then it appears in yellow once again in the centre of the field.

Target

The target platform / device is Xilinx Spartan-3E FPGA

Milestones

Week	Outline	What is Due?
9	Project #2 description and specs.	
10	VHDL code and compilation	The symbol and block diagram.
11	Hardware integration with VGA	Static video frame demonstration.
12	Final project preparation.	Complete project demonstration.

Supplementary Material

VGA Specifications

All horizontal (line) time periods are specified in multiples of the VGA pixel clock, which is 25 MHz for a 60 Hz refresh rate. All vertical (frame) time periods are specified in multiples of VGA lines.

Table I: VGA Horizontal Parameters

Parameter	Clock Cycles
Complete Line	800
Front Porch	16
Sync Pulse	96
Back Porch	48
Active image area	640

Table II: VGA Vertical Parameters

Parameter	Lines
Complete Frame	525
Front Porch	10
Sync Pulse	2
Back Porch	33
Active image area	480

VGA Interface Pin Constraints

The following are physical pin constraints for the VGA interface available on the Laboratory boards.

```
# 50 MHz input clock.
NET “clk” LOC = “c9”;

# Synchronization signals.
NET "H"  LOC = "c5";
NET "V"  LOC = "d5";

# Pixel clock for the video DAC.
NET "DAC_CLK"  LOC = "a4";

# Blue channel pins.
NET "Bout<7>"  LOC = "b16";
NET "Bout<6>"  LOC = "a16";
NET "Bout<5>"  LOC = "d14";
NET "Bout<4>"  LOC = "c14";
NET "Bout<3>"  LOC = "b14";
NET "Bout<2>"  LOC = "a14";
NET "Bout<1>"  LOC = "b13";
NET "Bout<0>"  LOC = "a13";

# Green channel pins.
NET "Gout<0>"  LOC = "f9";
NET "Gout<1>"  LOC = "e9";
NET "Gout<2>"  LOC = "d11";
NET "Gout<3>"  LOC = "c11";
NET "Gout<4>"  LOC = "f11";
NET "Gout<5>"  LOC = "e11";
NET "Gout<6>"  LOC = "e12";
NET "Gout<7>"  LOC = "f12";

# Red channel pins.
NET "Rout<0>"  LOC = "a6";
NET "Rout<1>"  LOC = "b6";
NET "Rout<2>"  LOC = "e7";
NET "Rout<3>"  LOC = "f7";
NET "Rout<4>"  LOC = "d7";
NET "Rout<5>"  LOC = "c7";
NET "Rout<6>"  LOC = "f8";
NET "Rout<7>"  LOC = "e8";
```

```
# On-board switches.
NET "SW0"  LOC = "N17";
NET "SW1"  LOC = "H18";
NET "SW2"  LOC = "L14";
NET "SW3"  LOC = "L13";
```